Very Low-power, 16-bit & 20-bit A/D Converters

Features

- Very Low Power Consumption
  - Single supply +5 V operation: 1.7 mW
  - Dual supply ±5 V operation: 3.2 mW
- Offers superior performance to VFCs and multi-slope integrating ADCs
- Differential Inputs
  - Single Channel (CS5507/8) and Four-Channel (CS5505/6) pseudo-differential versions
- Either 5 V or 3.3 V Digital Interface
- Linearity Error:
  - ±0.0015% FS (16-bit CS5505/7)
  - ±0.0007% FS (20-bit CS5506/8)
- Output update rates up to 100 Sps
- Flexible Serial Port
- Pin-Selectable Unipolar/Bipolar Ranges

Description

The CS5505/6/7/8 are a family of low power CMOS A/D converters which are ideal for measuring low-frequency signals representing physical, chemical, and biological processes.

The CS5507/8 have single-channel differential analog and reference inputs while the CS5505/6 have four pseudo-differential analog input channels. The CS5505/7 have a 16-bit output word. The CS5506/8 have a 20-bit output word. The CS5505/6/7/8 sample upon command up to 100 Sps.

The on-chip digital filter offers superior line rejection at 50 and 60 Hz when the device is operated from a 32.768 kHz clock (output word rate = 20 Sps).

The CS5505/6/7/8 include on-chip self-calibration circuitry which can be initiated at any time or temperature to ensure minimum offset and full-scale errors.

The CS5505/6/7/8 serial port offers two general-purpose modes for the direct interface to shift registers or synchronous serial ports of industry-standard microcontrollers.

ORDERING INFORMATION
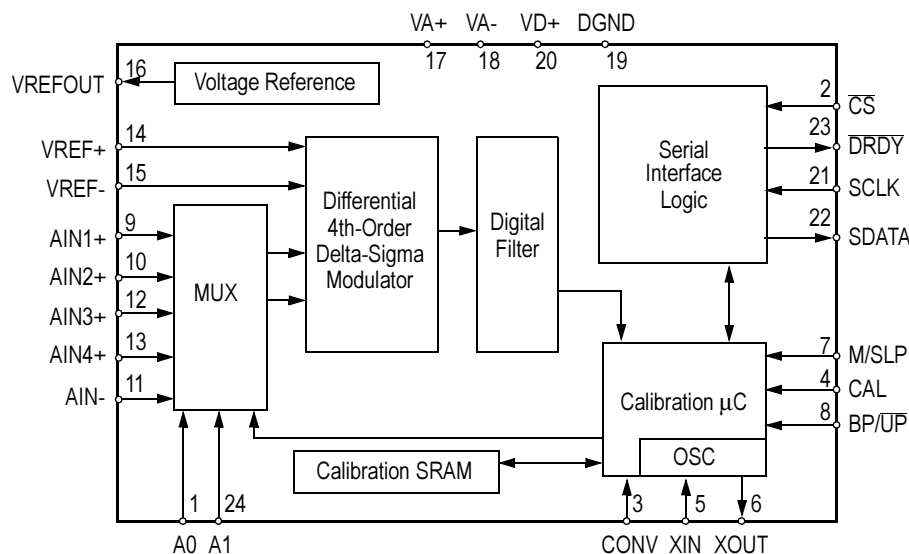
CS5505 (16-BIT) AND CS5506 (20-BIT) SHOWN

ANALOG CHARACTERISTICS $(T_A = T_{MIN}$ to T_{MAX}; VA+ = 5V $\pm$ 10%; VA- = -5V $\pm$ 10%; VD+ = 3.3V $\pm$ 5%; VREF+ = 2.5V(external); VREF- = 0V; f_{CLK} = 32.768kHz; Bipolar Mode; R_{source} = 1kΩ with a 10nF to AGND at AIN; Analog input channel AIN1+; AIN- = AGND; unless otherwise specified.) (Notes 1, 2)

Parameter*		CS5505/7-A				Units
		Min	Typ	Max		
Specified Temperature Range			-40 to +85			$^\circ$C
Accuracy						
Linearity Error		-	0.0015	0.003		$\pm$%FS
Differential Nonlinearity		-	$\pm$0.25	$\pm$0.5		LSB_{16}
Full Scale Error	(Note 3)	-	$\pm$0.25	$\pm$2		LSB_{16}
Full Scale Drift	(Note 4)	-	$\pm$0.5	-		LSB_{16}
Unipolar Offset	(Note 3)	-	$\pm$0.5	$\pm$2		LSB_{16}
Unipolar Offset Drift	(Note 4)	-	$\pm$0.5	-		LSB_{16}
Bipolar Offset	(Note 3)	-	$\pm$0.25	$\pm$1		LSB_{16}
Bipolar Offset Drift	(Note 4)	-	$\pm$0.25	-		LSB_{16}
Noise (Referred to Output)		-	0.16	-		LSB-rms$_{16}$

Notes: 1. The AIN pin presents a very high input resistance at dc and a minor dynamic load which scales to the master clock frequency. Both source resistance and shunt capacitance are therefore critical in determining the CS5505/6/7/8's source impedance requirements. For more information refer to the text section *Analog Input Impedance Considerations.*

2. Specifications guaranteed by design, characterization and/or test.

3. Applies after calibration at the temperature of interest.

4. Total drift over the specified temperature range since calibration at power-up at 25°C. Recalibration at any temperature will remove these errors.

	Unipolar Mode			Bipolar Mode		
mV	LSB's	% FS	ppm FS	LSB's	% FS	ppm FS
10	0.26	0.0004	4	0.13	0.0002	2
19	0.50	0.0008	8	0.26	0.0004	4
38	1.00	0.0015	15	0.50	0.0008	8
76	2.00	0.0030	30	1.00	0.0015	15
152	4.00	0.0061	61	2.00	0.0030	30

VREF = 2.5V

CS5505/7; 16-Bit Unit Conversion Factors

* Refer to the Specification Definitions immediately following the Pin Description Section.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (T_A = T_{MIN} to T_{MAX}; VA+ = 5V $\pm$ 10%; VA- = -5V $\pm$ 10%; VD+ = 3.3V $\pm$ 5%; VREF+ = 2.5V (external); VREF- = 0V; f_{CLK} = 32.768kHz; Bipolar Mode; R_{source} = 1kΩ with a 10nF to AGND at AIN; Analog input channel AIN1+; AIN- = AGND; unless otherwise specified.) (Notes 1, 2)

Parameter*		CS5506/8-B				Units
		Min	Typ	Max		
Specified Temperature Range		-40 to +85				$^\circ$C
Accuracy						
Linearity Error		-	0.0007	0.0015		$\pm$%FS
Differential Nonlinearity (No Missing Codes)		20	-	-		Bits
Full Scale Error	(Note 3)	-	$\pm$4	$\pm$32		LSB_{20}
Full Scale Drift	(Note 4)	-	$\pm$8	-		LSB_{20}
Unipolar Offset	(Note 3)	-	$\pm$8	$\pm$32		LSB_{20}
Unipolar Offset Drift	(Note 4)	-	$\pm$8	-		LSB_{20}
Bipolar Offset	(Note 3)	-	$\pm$4	$\pm$16		LSB_{20}
Bipolar Offset Drift	(Note 4)	-	$\pm$4	-		LSB_{20}
Noise (Referred to Output)		-	2.6	-		$LSB\text{-}rms_{20}$

	Unipolar Mode			Bipolar Mode		
mV	LSB's	% FS	ppm FS	LSB's	% FS	ppm FS
0.596	0.25	0.0000238	0.24	0.13	0.0000119	0.12
1.192	0.50	0.0000477	0.47	0.26	0.0000238	0.24
2.384	1.00	0.0000954	0.95	0.50	0.0000477	0.47
4.768	2.00	0.0001907	1.91	1.00	0.0000954	0.95
9.537	4.00	0.0003814	3.81	2.00	0.0001907	1.91

VREF = 2.5V

CS5506/8; 20-Bit Unit Conversion Factors

DYNAMIC CHARACTERISTICS

Parameter	Symbol	Ratio	Units
Modulator Sampling Frequency	f_S	$f_{clk}/2$	Hz
Output Update Rate (CONV = 1)	f_{out}	$f_{clk}/1622$	Sps
Filter Corner Frequency	f_{-3dB}	$f_{clk}/1928$	Hz
Settling Time to $\frac{1}{2}$ LSB (FS Step)	t_S	$1/f_{out}$	s

ANALOG CHARACTERISTICS (T_A = T_{MIN} to T_{MAX}; VA+ = 5V ± 10%; VA- = -5V ± 10%; VD+ = 3.3V ± 5%; VREF+ = 2.5V (external); VREF- = 0V; f_{CLK} = 32.768kHz; Bipolar Mode; R_{SOURCE} = 1kΩ with a 10nF to AGND at AIN; Analog input channel AIN1+; AIN- = AGND; unless otherwise specified.) (Notes 1, 2)

Parameter*	CS5505/7 CS5506/8				Units
	Min	Typ	Max		
Specified Temperature Range		-40 to +85			°C
Analog Input					
Analog Input Range: Unipolar (VAIN+)-(VAIN-) Bipolar (Note 5)		0 to +2.5 ±2.5			Volts Volts
Common Mode Rejection: dc 50, 60 Hz (Note 6)	- 120	105 -	- -		dB dB
Off Channel Isolation	-	120	-		dB
Input Capacitance	-	15	-		pF
DC Bias Current (Note 1)	-	5	-		nA
Voltage Reference (Output)					
VREFOUT Voltage	-	(VA+)-2.5	-		Volts
VREFOUT Voltage Tolerance	-	-	4.0		%
VREFOUT Voltage Temperature Coefficient	-	60	-		ppm/°C
VREFOUT Line Regulation	-	1.5	-		mV/Volt
VREFOUT Output Voltage Noise 0.1 to 10 Hz	-	50	-		μVp-p
VREFOUT: Source Current Sink Current	- -	- -	3 50		μA μA
Power Supplies					
DC Power Supply Currents: I_{Total} I_{Analog} $I_{Digital}$	- - -	340 300 40	450 - -		μA μA μA
Power Dissipation: (Note 7) SLEEP inactive SLEEP active	- -	3.2 5	4.5 10		mW μW
Power Supply Rejection: Positive Supplies Negative Supplies	- -	80 80	- -		dB dB

Notes: 5. Common mode voltage may be at any value as long as AIN+ and AIN- remain within the VA+ and VA- supply voltages.
       6. XIN = 32.768 kHz. Guaranteed by design and / or characterization.
       7. All outputs unloaded. All inputs CMOS levels. SLEEP mode controlled by M/SLP pin.
          SLEEP active = M/SLP pin at (VD+)/2 input level.

5V DIGITAL CHARACTERISTICS (T_A = T_{MIN} to T_{MAX}; VA+VD+ = 5V ± 10%; VA-= -5V ± 10%; DGND = 0.) All measurements below are performed under static conditions. (Note 2)

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage:	XIN	V_{IH}	3.5	-	-	V
	M/SLP	V_{IH}	0.9VD+	-	-	V
	All Pins Except XIN and M/SLP	V_{IH}	2.0	-	-	V
Low-Level Input Voltage:	XIN	V_{IL}	-	-	1.5	V
	M/SLP	V_{IL}	-	-	0.1VD+	V
	All Pins Except XIN and M/SLP	V_{IL}	-	-	0.8	V
M/SLP SLEEP Active Threshold	(Note 8)	V_{SLP}	0.45VD+	0.5VD+	0.55VD+	V
High-Level Output Voltage	(Note 9)	V_{OH}	(VD+)-1.0	-	-	V
Low Level Output Voltage I_{out} = 1.6 mA		V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-	1	10	μA
3-State Leakage Current		I_{OZ}	-	-	±10	μA
Digital Output Pin Capacitance		C_{out}	-	9	-	pF

Notes: 8. Under normal operation this pin should be tied to VD+ or DGND. Anytime the voltage on the M/SLP pin enters the SLEEP active threshold range the device will enter the power down condition. Returning to the active state requires elapse of the power-on reset period, the oscillator to start-up, and elapse of the wake-up period.

9. I_{out} = -100 μA. This guarantees the ability to drive one TTL load. (V_{OH} = 2.4V @ I_{out} = -40 μA).

3.3V DIGITAL CHARACTERISTICS (T_A = T_{MIN} to T_{MAX}; VA+ = 5V ± 10%; VD+ = 3.3V ± 5%; VA-= -5V ± 10%; DGND = 0.) All measurements below are performed under static conditions. (Note 2)

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage:	XIN	V_{IH}	0.7VD+	-	-	V
	M/SLP	V_{IH}	0.9VD+	-	-	V
	All Pins Except XIN and M/SLP	V_{IH}	0.6VD+	-	-	V
Low-Level Input Voltage:	XIN	V_{IL}	-	-	0.3VD+	V
	M/SLP	V_{IL}	-	-	0.1VD+	V
	All Pins Except XIN and M/SLP	V_{IL}	-	-	0.16VD+	V
M/SLP SLEEP Active Threshold	(Note 8)	V_{SLP}	0.43VD+	0.45VD+	0.47VD+	V
High-Level Output Voltage I_{out} = -400 μA		V_{OH}	(VD+)-0.3	-	-	V
Low Level Output Voltage I_{out} = 400 μA		V_{OL}	-	-	0.3	V
Input Leakage Current		I_{in}	-	1	10	μA
3-State Leakage Current		I_{OZ}	-	-	±10	μA
Digital Output Pin Capacitance		C_{out}	-	9	-	pF

5V SWITCHING CHARACTERISTICS $(T_A = T_{MIN}$ to T_{MAX}; VA+, VD+ = 5V $\pm$ 10%;

VA- = -5V $\pm$ 10%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF.) (Note 2)

Parameter			Symbol	Min	Typ	Max	Units
Master Clock Frequency:	Internal Oscillator:		XIN	30.0	32.768	53.0	kHz
	External Clock:		f_{clk}	30	-	163	kHz
Master Clock Duty Cycle				40	-	60	%
Rise Times:	Any Digital Input	(Note 10)	t_{rise}	-	-	1.0	µs
	Any Digital Output			-	50	-	ns
Fall Times:	Any Digital Input	(Note 10)	t_{fall}	-	-	1.0	µs
	Any Digital Output			-	20	-	ns
Start-Up							
Power-On Reset Period		(Note 11)	t_{res}	-	10	-	ms
Oscillator Start-up Time	XTAL=32.768 kHz	(Note 12)	t_{osu}	-	500	-	ms
Wake-up Period		(Note 13)	t_{wup}	-	$1800/f_{clk}$	-	s
Calibration							
CONV Pulse Width (CAL = 1)		(Note 14)	t_{ccw}	100	-	-	ns
CONV and CAL High to Start of Calibration			t_{scl}	-	-	$2/f_{clk}+200$	ns
Start of Calibration to End of Calibration			t_{cal}	-	$3246/f_{clk}$	-	s
Conversion							
Set Up Time	A0, A1 to CONV High		t_{sac}	50	-	-	ns
Hold Time	A0, A1 after CONV High		t_{hca}	100	-	-	ns
CONV Pulse Width			t_{cpw}	100	-	-	ns
CONV High to Start of Conversion			t_{scn}	-	-	$2/f_{clk}+200$	ns
Set Up Time	BP/UP stable prior to DRDY falling		t_{bus}	$82/f_{clk}$	-	-	s
Hold Time	BP/UP stable after DRDY falls		t_{buh}	0	-	-	ns
Start of Conversion to End of Conversion		(Note 15)	t_{con}	-	$1624/f_{clk}$	-	s

Notes: 10. Specified using 10% and 90% points on waveform of interest.
11. An internal power-on-reset is activated whenever power is applied to the device, or when coming out of a SLEEP state.
12. Oscillator start-up time varies with the crystal parameters. This specification does not apply when using an external clock source.
13. The wake-up period begins once the oscillator starts;
or when using an external f_{clk}, after the power-on reset time elapses.
14. Calibration can also be initiated by pulsing CAL high while CONV=1.
15. Conversion time will be $1622/f_{clk}$ if CONV remains high continuously.

3.3V SWITCHING CHARACTERISTICS (T$_A$ = T$_{MIN}$ to T$_{MAX}$ VA+ = 5V $\pm$ 10%;

VD+ = 3.3V $\pm$ 5%; VA- = -5V $\pm$ 10%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; CL = 50 pF.) (Note 2)

Parameter			Symbol	Min	Typ	Max	Units
Master Clock Frequency:	Internal Oscillator:		XIN	30.0	32.768	53.0	kHz
	External Clock:		f$_{clk}$	30	-	163	kHz
Master Clock Duty Cycle				40	-	60	%
Rise Times:	Any Digital Input	(Note 10)	t$_{rise}$	-	-	1.0	μs
	Any Digital Output			-	50	-	ns
Fall Times:	Any Digital Input	(Note 10)	t$_{fall}$	-	-	1.0	μs
	Any Digital Output			-	20	-	ns
Start-Up							
Power-On Reset Period		(Note 11)	t$_{res}$	-	10	-	ms
Oscillator Start-up Time	XTAL=32.768 kHz	(Note 12)	t$_{osu}$	-	500	-	ms
Wake-up Period		(Note 13)	t$_{wup}$	-	1800/f$_{clk}$	-	s
Calibration							
CONV Pulse Width (CAL = 1)		(Note 14)	t$_{ccw}$	100	-	-	ns
CONV and CAL High to Start of Calibration			t$_{scl}$	-	-	2/f$_{clk}$+200	ns
Start of Calibration to End of Calibration			t$_{cal}$	-	3246/f$_{clk}$	-	s
Conversion							
Set Up Time	A0, A1 to CONV High		t$_{sac}$	50	-	-	ns
Hold Time	A0, A1 after CONV High		t$_{hca}$	100	-	-	ns
CONV Pulse Width			t$_{cpw}$	100	-	-	ns
CONV High to Start of Conversion			t$_{scn}$	-	-	2/f$_{clk}$+200	ns
Set Up Time	BP/UP stable prior to DRDY falling		t$_{bus}$	82/f$_{clk}$	-	-	s
Hold Time	BP/UP stable after DRDY falls		t$_{buh}$	0	-	-	ns
Start of Conversion to End of Conversion		(Note 15)	t$_{con}$	-	1624/f$_{clk}$	-	s

Figure 1. Calibration Timing (Not to Scale)
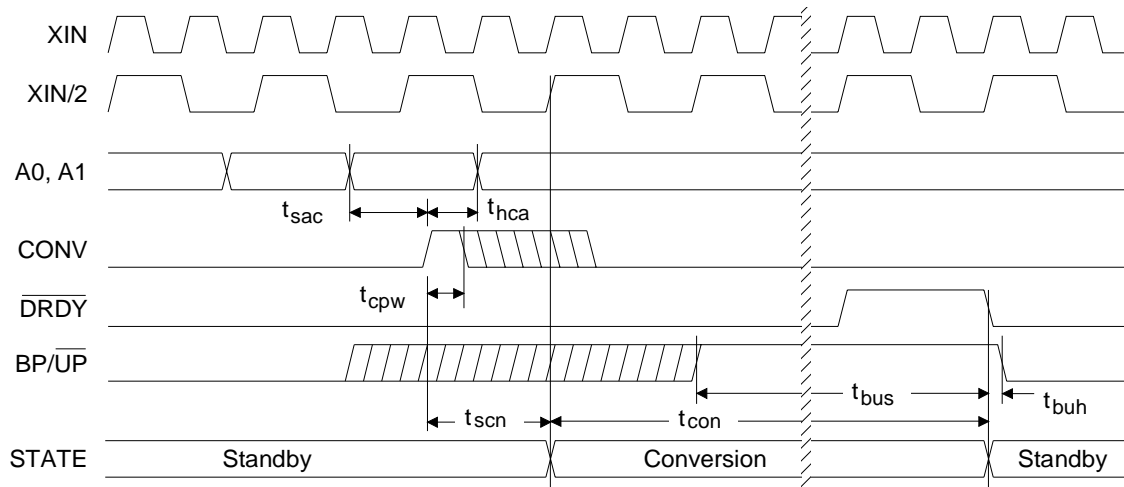
Figure 2. Conversion Timing (Not to Scale)

5V SWITCHING CHARACTERISTICS $(T_A = T_{MIN}$ to $T_{MAX};$ VA+, VD+ = 5V $\pm$ 10%;

VA- = -5V $\pm$ 10%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF.) (Note 2)

Parameter		Symbol	Min	Typ	Max	Units
SSC Mode (M/SLP = VD+)						
Access Time:	CS Low to SDATA out (DRDY = low)	t_{csd1}	-	-	$2/f_{clk}$	ns
	DRDY falling to MSB (CS = low)	t_{dfd}	-	$2/f_{clk}$	$3/f_{clk}$	ns
SDATA Delay Time:	SCLK falling to next SDATA bit	t_{dd1}	-	80	250	ns
SCLK Delay Time	SDATA MSB bit to SCLK rising	t_{cd1}	-	$1/f_{clk}$	-	ns
Serial Clock (Out)	Pulse Width High	t_{ph1}	-	$1/f_{clk}$	-	ns
	Pulse Width Low	t_{pl1}	-	$1/f_{clk}$	-	ns
Output Float Delay:	CS high to output Hi-Z (Note 16)	t_{fd1}	-	-	$2/f_{clk}$	ns
	SCLK rising to SDATA Hi-Z	t_{fd2}	-	$1/f_{clk}$	-	ns
SEC Mode (M/SLP = DGND)						
Serial Clock (In)		f_{sclk}	0	-	2.5	MHz
Serial Clock (In)	Pulse Width High	t_{ph2}	200	-	-	ns
	Pulse Width Low	t_{pl2}	200	-	-	ns
Access Time:	CS Low to data valid (Note 17)	t_{csd2}	-	60	200	ns
Maximum Delay time:	(Note 18)					
	SCLK falling to new SDATA bit	t_{dd2}	-	150	310	ns
Output Float Delay:	CS high to output Hi-Z (Note 16)	t_{fd3}	-	60	150	ns
	SCLK falling to SDATA Hi-Z	t_{fd4}	-	160	300	ns

Notes: 16. If $\overline{CS}$ is returned high before all data bits are output, the SDATA and SCLK outputs will complete the current data bit and then go to high impedance.

17. If $\overline{CS}$ is activated asynchronously to $\overline{DRDY}$, $\overline{CS}$ will not be recognized if it occurs when $\overline{DRDY}$ is high for 2 clock cycles. The propagation delay time may be as great as 2 f_{clk} cycles plus 200 ns. To guarantee proper clocking of SDATA when using asynchronous $\overline{CS}$, SCLK(i) should not be taken high sooner than 2 f_{clk} + 200 ns after $\overline{CS}$ goes low.

18. SDATA transitions on the falling edge of SCLK. Note that a rising SCLK must occur to enable the serial port shifting mechanism before falling edges can be recognized.

3.3V SWITCHING CHARACTERISTICS (T_A = T_{MIN} to T_{MAX} VA+ = 5V $\pm$ 10%; VD+ = 3.3V $\pm$ 5%; VA- = -5V $\pm$ 10%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF.) (Note 2)

Parameter		Symbol	Min	Typ	Max	Units
SSC Mode (M/SLP = VD+)						
Access Time:	CS Low to SDATA out (DRDY = low)	t_{csd1}	-	-	2/fclk	ns
	DRDY falling to MSB (CS = low)	t_{dfd}	-	2/f_{clk}	3/f_{clk}	ns
SDATA Delay Time:	SCLK falling to next SDATA bit	t_{dd1}	-	265	400	ns
SCLK Delay Time	SDATA MSB bit to SCLK rising	t_{cd1}	-	1/f_{clk}	-	ns
Serial Clock (Out)	Pulse Width High	t_{ph1}	-	1/f_{clk}	-	ns
	Pulse Width Low	t_{pl1}	-	1/f_{clk}	-	ns
Output Float Delay:	CS high to output Hi-Z (Note 16)	t_{fd1}	-	-	2/f_{clk}	ns
	SCLK rising to SDATA Hi-Z	t_{fd2}	-	1/f_{clk}	-	ns
SEC Mode (M/SLP = DGND)						
Serial Clock (In)		f_{sclk}	0	-	1.25	MHz
Serial Clock (In)	Pulse Width High	t_{ph2}	200	-	-	ns
	Pulse Width Low	t_{pl2}	200	-	-	ns
Access Time:	CS Low to data valid (Note 17)	t_{csd2}	-	100	200	ns
Maximum Delay time:	(Note 18)					
	SCLK falling to new SDATA bit	t_{dd2}	-	400	600	ns
Output Float Delay:	CS high to output Hi-Z (Note 16)	t_{fd3}	-	70	150	ns
	SCLK falling to SDATA Hi-Z	t_{fd4}	-	320	500	ns
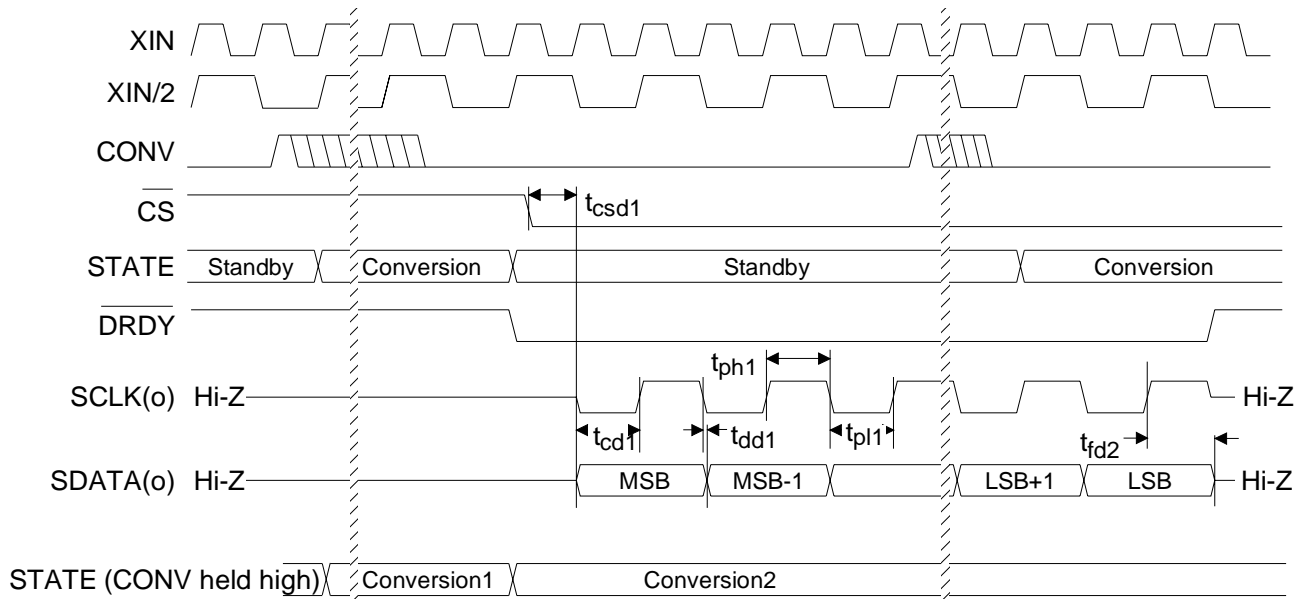
Figure 3. Timing Relationships; SSC Mode (Not to Scale)
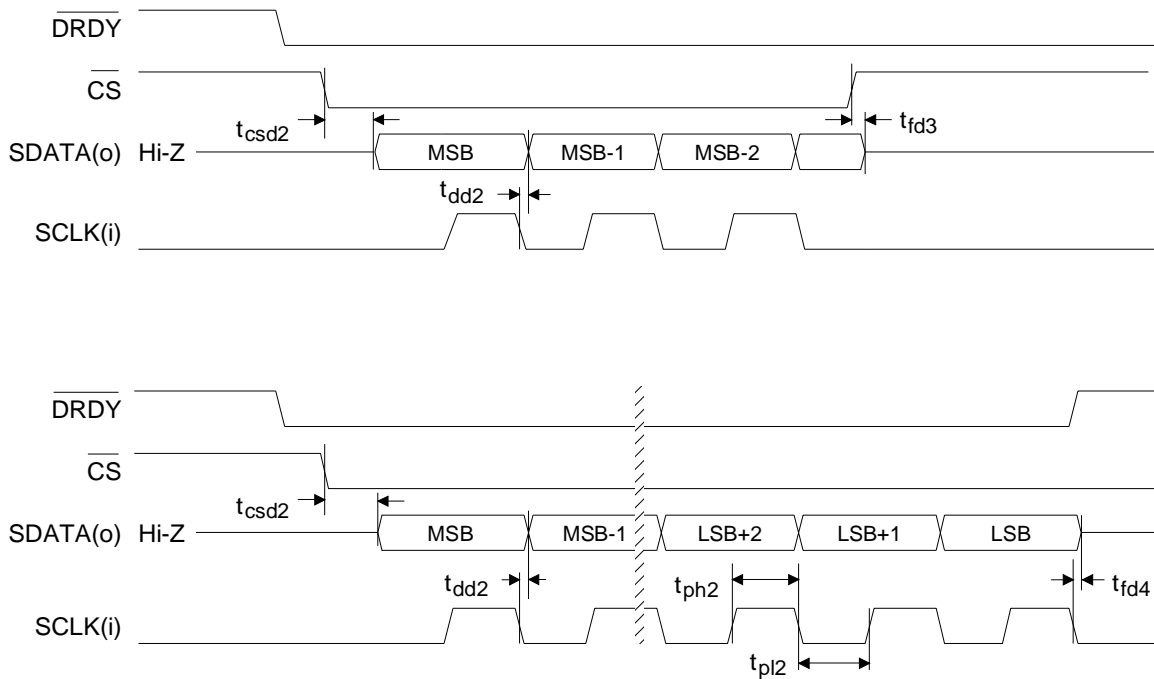
Figure 4. Timing Relationships; SEC Mode (Not to Scale)

RECOMMENDED OPERATING CONDITIONS (DGND = 0V) (Note 19)

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies: Positive Digital	VD+	3.15	5.0	5.5	V
(VA+)-(VA-)	V$_{diff}$	4.5	10	11	V
Positive Analog	VA+	4.5	5.0	11	V
Negative Analog	VA-	0	-5.0	-5.5	V
Analog Reference Voltage (Note 20)	(VREF+)-(VREF-)	1.0	2.5	3.6	V
Analog Input Voltage: (Note 21)					
Unipolar	VAIN	0	-	(VREF+)-(VREF-)	V
Bipolar	VAIN	-((VREF+)-(VREF-))	-	+((VREF+)-(VREF-))	V

Notes: 19. All voltages with respect to ground.
     20. The CS5505/6/7/8 can be operated with a reference voltage as low as 100 mV; but with a corresponding reduction in noise-free resolution. The common mode voltage of the voltage reference may be any value as long as +VREF and -VREF remain inside the supply values of VA+ and VA-.
     21. The CS5505/6/7/8 can accept input voltages up to the analog supplies (VA+ and VA-). In unipolar mode the CS5505/6/7/8 will output all 1's if the dc input magnitude ((AIN+)-(AIN-)) exceeds ((VREF+)-(VREF-)) and will output all 0's if the input becomes more negative than 0 Volts.
In bipolar mode the CS5505/6/7/8 will output all 1's if the dc input magnitude ((AIN+)-(AIN-)) exceeds ((VREF+)-(VREF-)) and will output all 0's if the input becomes more negative in magnitude than -((VREF+)-(VREF-)).

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies: Digital Ground (Note 22)	DGND	-0.3	-	(VD+)-0.3	V
Positive Digital (Note 23)	VD+	-0.3	-	6.0 or VA+	V
Positive Analog	VA+	-0.3	-	12.0	V
Negative Analog	VA-	+0.3	-	-6.0	V
(VA+)-(VA-)	V$_{diff1}$	-0.3	-	12.0	V
(VA+)-(VD+)	V$_{diff2}$	-0.3	-	12.0	V
Input Current, Any Pin Except Supplies (Notes 24, 25)	I$_{in}$	-	-	±10	mA
Analog Input Voltage AIN and VREF pins	V$_{INA}$	(VA-)-0.3	-	(VA+)+0.3	V
Digital Input Voltage	V$_{IND}$	-0.3	-	(VD+)+0.3	V
Ambient Operating Temperature	T$_A$	-55	-	125	°C
Storage Temperature	T$_{stg}$	-65	-	150	°C

Notes: 22. No pin should go more positive than (VA+)+0.3V.
     23. VD+ must always be less than (VA+)+0.3 V,and can never exceed 6.0V.
     24. Applies to all pins including continuous overvoltage conditions at the analog input (AIN) pin.
     25. Transient currents of up to 100mA will not cause SCR latch-up. Maximum input current for a power supply pin is ± 50 mA.

* WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

GENERAL DESCRIPTION

The CS5505/6/7/8 are very low power monolithic CMOS A/D converters designed specifically for measurement of dc signals. The CS5505/7 are 16-bit converters (a four channel and a single channel version). The CS5506/8 are 20-bit converters (a four channel and a single channel version). Each of the devices includes a delta-sigma charge-balance converter, a voltage reference, a calibration microcontroller with SRAM, a digital filter and a serial interface. The CS5505 and CS5506 include a four channel pseudo-differential (all four channels have the same reference measurement node) multiplexer.

The CS5505/6/7/8 include an on-chip reference but can also utilize an off-chip reference for precision applications. The CS5505/6/7/8 can be used to measure either unipolar or bipolar signals. The devices use self-calibration to insure excellent offset and gain accuracy.

The CS5505/6/7/8 are optimized to operate from a 32.768 kHz crystal but can be driven by an external clock whose frequency is between 30 kHz and 163 kHz. When the digital filter is operated with a 32.768 kHz clock, the filter has zeros precisely at 50 and 60 Hz line frequencies and multiples thereof.

The CS5505/6/7/8 use a "start convert" command to latch the input channel selection and to start a convolution cycle on the digital filter. Once the filter cycle is completed, the output port is updated. When operated with a 32.768 kHz clock the ADC converts and updates its output port at 20 samples/sec. The throughput rate per channel is the output update rate divided by the number of channels being multiplexed. The output port includes a serial interface with two modes of operation.

The CS5505/6/7/8 can operate from dual polarity power supplies (+5 and -5), from a single +5 volt supply, or with +10 volts on the analog and +5 on the digital. They can also operate with dual polarity (+5 and -5), or from a single +5 volt supply on the analog and + 3.3 on the digital.

THEORY OF OPERATION FOR THE CS5505/6/7/8

The front page of this data sheet illustrates the block diagram of the CS5505/6.

Basic Converter Operation

The CS5505/6/7/8 A/D converters have four operating states. These are start-up, calibration, conversion and sleep. When power is first applied, the device enters the start-up state. The first step is a power-on reset delay of about 10 ms which resets all of the logic in the device. To proceed with start-up, the oscillator must then begin oscillating. After the power-on reset the device enters the wake-up period for 1800 clock cycles after clock is present. This allows the delta-sigma modulator and other circuitry (which are operating with very low currents) to reach a stable bias condition prior to entering into either the calibration or conversion states. During the 1800 cycle wake-up period, the device can accept an input command. Execution of this command will not occur until the complete wake-up period elapses. If no command is given, the device enters the standby mode.

Calibration

After the initial application of power, the CS5505/6/7/8 must enter the calibration state prior to performing accurate conversions. During calibration, the chip executes a two-step process. The device first performs an offset calibration and then follows this with a gain calibration. The two calibration steps determine the zero reference point and the full scale reference point of the converter's transfer function. From these points it calibrates the zero point and a gain

slope to be used to properly scale the output digital codes when doing conversions.

The calibration state is entered whenever the CAL and CONV pins are high at the same time. The state of the CAL and CONV pins at power-on and when coming out of sleep are recognized as commands, but will not be executed until the end of the 1800 clock cycle wake-up period. Note that any time CONV transitions from low to high, the multiplexer inputs A0 and A1 are latched internal to the CS5505 and CS5506 devices. These latched inputs select the analog input channel which will be used once conversion commences.

If CAL and CONV become active (high) during the 1800 clock cycle wake-up time, the converter will wait until the wake-up period elapses before executing the calibration. If the wake-up time has elapsed, the converter will be in the standby mode waiting for instruction and will enter the calibration cycle immediately. The calibration lasts for 3246 clock cycles. Calibration coefficients are then retained in the SRAM (static RAM) for use during conversion.

At the end of the calibration cycle, the on-chip microcontroller checks the logic state of the CONV signal. If the CONV input is low the device will enter the standby mode where it waits for further instruction. If the CONV signal is high at the end of the calibration cycle, the converter will enter the conversion state and perform a conversion on the input channel which was selected when CONV transitioned from low to high. The CAL signal can be returned low any time after calibration is initiated. CONV can also be returned low, but it should never be taken low and then taken back high until the calibration period has ended and the converter is in the standby state. If CONV is taken low and then high again with CAL high while the converter is calibrating, the device will interrupt the current calibration cycle and start a new one. If CAL is taken low and CONV is taken low and

then high during calibration, the calibration cycle will continue as the conversion command is disregarded. The states of A0, A1 and BP/$\overline{\text{UP}}$ are not important during calibrations.

If an "end of calibration" signal is desired, pulse the CAL signal high while leaving the CONV signal high continuously. Once the calibration is completed, a conversion will be performed. At the end of the conversion, $\overline{\text{DRDY}}$ will fall to indicate the first valid conversion after the calibration has been completed.

See Understanding Converter Calibration for details on how the converter calibrates its transfer function.

Conversion

The conversion state can be entered at the end of the calibration cycle, or whenever the converter is idle in the standby mode. If CONV is taken high to initiate a calibration cycle (CAL also high), and remains high until the calibration cycle is completed (CAL is taken low after CONV transitions high), the converter will begin a conversion upon completion of the calibration period. The device will perform a conversion on the input channel selected by the A0 and A1 inputs when CONV transitioned high. Table 1 indicates the multiplexer channel selection truth table for A0 and A1.

A1	A0	Channel addressed
0	0	AIN1
0	1	AIN2
1	0	AIN3
1	1	AIN4

Table 1. Multiplexer Truth Table

The A0 and A1 inputs are latched internal to the 4-channel devices (CS5505/6) when CONV rises. A0 and A1 have internal pull-down circuits which default the multiplexer to channel

AIN1. The BP/$\overline{\text{UP}}$ pin is not a latched input. The BP/$\overline{\text{UP}}$ pin controls how the output word from the digital filter is processed. In bipolar mode the output word computed by the digital filter is offset by 8000H in the 16-bit CS5505/7 or 80000H in 20-bit CS5506/8 (see Understanding Converter Calibration). BP/$\overline{\text{UP}}$ can be changed after a conversion is started as long as it is stable for 82 clock cycles of the conversion period prior to $\overline{\text{DRDY}}$ falling. If one wishes to intermix measurement of bipolar and unipolar signals on various input channels, it is best to switch the BP/$\overline{\text{UP}}$ pin immediately after $\overline{\text{DRDY}}$ falls and leave BP/$\overline{\text{UP}}$ stable until $\overline{\text{DRDY}}$ falls again. If the converter is beginning a conversion starting from the standby state, BP/$\overline{\text{UP}}$ can be changed at the same time as A0 and A1.

The digital filter in the CS5505/6/7/8 has a Finite Impulse Response and is designed to settle to full accuracy in one conversion time. Therefore, the multiplexer can be changed at the conversion rate.

If CONV is left high, the CS5505/6/7/8 will perform continuous conversions on one channel. The conversion time will be 1622 clock cycles. If conversion is initiated from the standby state, there may be up to two XIN clock cycles of uncertainty as to when conversion actually begins. This is because the internal logic operates at one half the external clock rate and the exact phase of the internal clock may be 180° out of phase relative to the XIN clock. When a new conversion is initiated from the standby state, it will take up to two XIN clock cycles to begin. Actual conversion will use 1624 clock cycles before $\overline{\text{DRDY}}$ goes low to indicate that the serial port has been updated. See the Serial Interface Logic section of the data sheet for information on reading data from the serial port.

In the event the A/D conversion command (CONV going positive) is issued during the conversion state, the current conversion will be terminated and a new conversion will be initiated.

Voltage Reference

The CS5505/6/7/8 uses a differential voltage reference input. The positive input is VREF+ and the negative input is VREF-. The voltage between VREF+ and VREF- can range from 1 volt minimum to 3.6 volts maximum. The gain slope will track changes in the reference without recalibration, accommodating ratiometric applications.

The CS5505/6/7/8 include an on-chip voltage reference which outputs 2.5 volts on the VREFOUT pin. This voltage is referenced to the VA+ pin and will track changes relative to VA+. The VREFOUT output requires a 0.1 μF capacitor connected between VREFOUT and VA+ for stability. When using the internal reference, the VREFOUT signal should be connected to the VREF- input and the VREF+ pin should be connected to the VA+ supply. The internal voltage reference is capable of sourcing 3 μA maximum and sinking 50 μA maximum. If a more precise reference voltage is required, an external voltage reference should be used. If an external voltage reference is used, the VREFOUT pin of the internal reference should be connected directly to VA-. It cannot be left open unless the 0.1 μF capacitor is in place for stability.
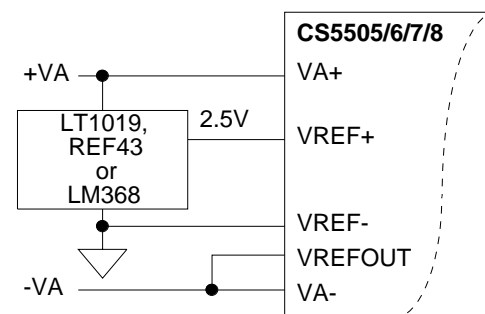
Figure 5. External Reference Connections
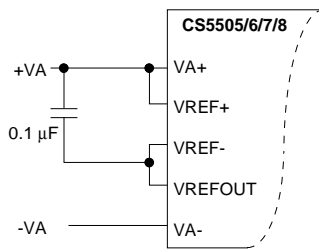
Figure 6. Internal Reference Connections

External reference voltages can range from 1.0 volt minimum to 3.6 volts maximum. The common mode voltage range of the external reference can allow the reference to lie at any voltage between the VA+ and VA- supply rails. Figures 5 and 6 illustrate how the CS5505/6/7/8 converters are connected for external and for internal voltage reference use, respectively.

Analog Input Range

The analog input range is set by the magnitude of the voltage between the VREF+ and VREF- pins. In unipolar mode the input range will equal the magnitude of the voltage reference. In bipolar mode the input voltage range will equate to plus and minus the magnitude of the voltage reference. While the voltage reference can be as great as 3.6 volts, its common mode voltage can be any value as long as the reference inputs VREF+ and VREF- stay within the supply volt-

ages for the A/D. The differential input voltage can also have any common mode value as long as the maximum signal magnitude stays within the supply voltages.

The A/D converter is intended to measure dc or low frequency inputs. It is designed to yield accurate conversions even with noise exceeding the input voltage range as long as the spectral components of this noise will be filtered out by the digital filter. For example, with a 3.0 volt reference in unipolar mode, the converter will accurately convert an input dc signal up to 3.0 volts with up to 15% overrange for 60 Hz noise. A 3.0 volt dc signal could have a 60 Hz component which is 0.5 volts above the maximum input of 3.0 (3.5 volts peak; 3.0 volts dc plus 0.5 volts peak noise) and still accurately convert the input signal (XIN = 32.768 kHz). This assumes that the signal plus noise amplitude stays within the supply voltages.

The CS5505/6/7/8 converters output data in binary format when converting unipolar signals and in offset binary format when converting bipolar signals. Table 2 outlines the output coding for the 16-bit CS5505/7 and the 20-bit CS5506/8 in both unipolar and bipolar measurement modes.

CS5505 and CS5507 (16 Bit)			CS5506 and CS5508 (20 Bit)		
Unipolar Input Voltage	Output Codes	Bipolar Input Voltage	Unipolar Input Voltage	Output Codes	Bipolar Input Voltage
>(VREF - 1.5 LSB)	**FFFF**	>(VREF - 1.5 LSB)	>(VREF - 1.5 LSB)	**FFFFF**	>(VREF - 1.5 LSB)
VREF - 1.5 LSB	**FFFF** **FFFE**	VREF - 1.5 LSB	VREF - 1.5 LSB	**FFFFF** **FFFFE**	VREF - 1.5 LSB
VREF/2 - 0.5 LSB	**8000** **7FFF**	-0.5 LSB	VREF/2 - 0.5 LSB	**80000** **7FFFF**	-0.5 LSB
+0.5 LSB	**0001** **0000**	-VREF + 0.5 LSB	+0.5 LSB	**00001** **00000**	-VREF + 0.5 LSB
<(+0.5 LSB)	**0000**	<(-VREF + 0.5 LSB)	<(+0.5 LSB)	**00000**	<(-VREF + 0.5 LSB)

Note: VREF = (VREF+) - (VREF-); Table excludes common mode voltage on the signal and reference inputs.

Table 2. Output Coding

Understanding Converter Calibration

Calibration can be performed at any time. A calibration sequence will minimize offset errors and set the gain slope scale factor. The delta-sigma modulator in the converter is a differential modulator. To calibrate out offset error, the converter internally connects the modulator differential inputs to an internal VREF- voltage and measures the 1's density output from the modulator. It stores the digital code representation for this 1's density in SRAM and remembers this code as being the zero scale point for the A/D conversion. The converter then connects the negative modulator differential input to the VREF- input and the positive modulator differential input to the VREF+ voltage. The 1's density output from the modulator is then recorded. The converter uses the digital representation of this 1's density along with the digital code for the zero scale point and calculates a gain scale factor. The gain scale factor is stored in SRAM and used for calculating the proper output codes during conversions.

The states of A0, A1 and BP/$\overline{\text{UP}}$ are ignored during calibration but should remain stable throughout the calibration period to minimize noise.

When conversions are performed in unipolar mode or in bipolar mode, the converter uses the same calibration factors to compute the digital output code. The only difference is that in bipolar mode the on-chip microcontroller offsets the computed output word by a code value of 8000H (16-bit) or 80000H (20-bit) and multiplies the LSB size by two. This means that the bipolar measurement range is not calibrated from full scale positive to full scale negative. Instead it is calibrated from the bipolar zero scale point to full scale positive. The slope factor is then extended below bipolar zero to accommodate the negative input signals. The converter can be used to convert both unipolar and bipolar signals by changing the BP/$\overline{\text{UP}}$ pin. Recalibration is not required when switching between unipolar and bipolar modes.

Converter Performance

The CS5505/6/7/8 A/D converters have excellent linearity performance. Calibration minimizes the errors in offset and gain. The CS5505/7 devices have no missing code performance to 16-bits. The CS5506/8 devices have no missing code performance to 20-bits. Figure 7 illustrates the DNL of the 16-bit CS5505. The converters achieve Common Mode Rejection (CMR) at dc of 105 dB typical, and CMR at 50 and 60 Hz of 120 dB typical.

The CS5505/6/7/8 can experience some drift as temperature changes. The CS5505/6/7/8 use chopper-stabilized techniques to minimize drift. Measurement errors due to offset or gain drift can be eliminated at any time by recalibrating the converter.
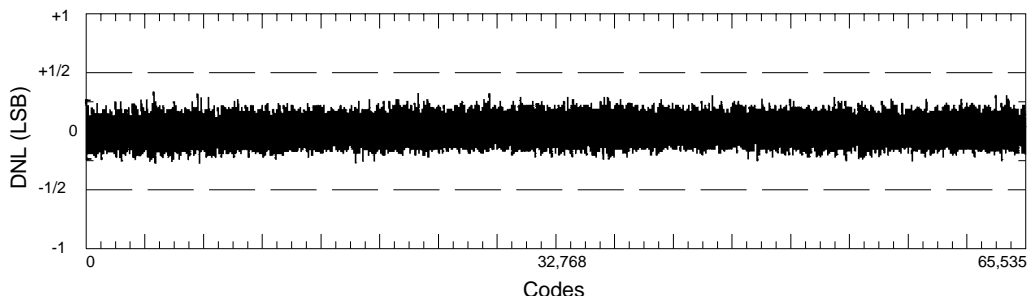
Figure 7. CS5505 Differential Nonlinearity plot.

Analog Input Impedance Considerations

The analog input of the CS5505/6/7/8 can be modeled as illustrated in Figure 8 (the model ignores the multiplexer switch resistance). Capacitors (15 pF each) are used to dynamically sample each of the inputs (AIN+ and AIN-). Every half XIN cycle the switch alternately connects the capacitor to the output of the buffer and then directly to the AIN pin. Whenever the sample capacitor is switched from the output of the buffer to the AIN pin, a small packet of charge (a dynamic demand of current) is required from the input source to settle the voltage of the sample capacitor to its final value. The voltage on the output of the buffer may differ up to 100 mV from the actual input voltage due to the offset voltage of the buffer. Timing allows one half of a XIN clock cycle for the voltage on the sample capacitor to settle to its final value. The equation which defines the settling time is:

$$V_e = V_{max}\, e^{-t/RC}$$

Where Ve is the final settled value, V_{max} is the maximum error voltage value of the input signal, R is the value of the input source resistance, C is the 15 pF sample capacitor plus the value of any stray or additional capacitance at the input pin. The value of t is equal to 1/(2XIN).
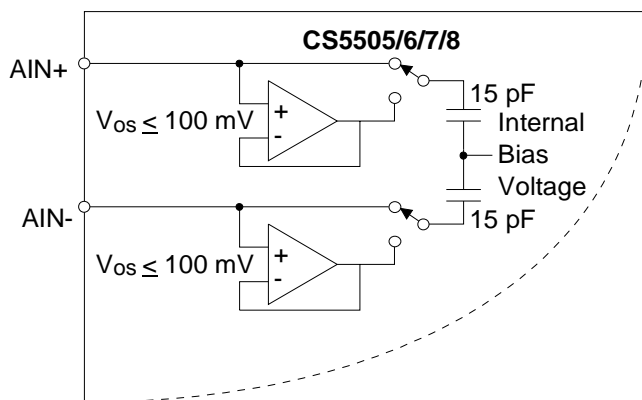
Figure 8. Analog Input Model

V_{max} occurs the instant the sample capacitor is switched from the buffer output to the AIN pin. Prior to switching, AIN has an error estimated as being less than or equal to V_e. V_{max} is equal to the prior error (V_e) plus the additional error from the buffer offset. The estimate for V_{max} is:

$$V_{max} = V_e + 100mV\, \frac{15pF}{(15pF + C_{EXT})}$$

Where C_{EXT} is the combination of any external or stray capacitance.

From the settling time equation, an equation for the maximum acceptable source resistance is derived.

$$Rs_{max} = \frac{-1}{2XIN\,(15pF + C_{EXT})\, \ln\left[\dfrac{V_e}{V_e + \dfrac{15pF(100mv)}{(15pF + C_{EXT})}}\right]}$$

This equation assumes that the offset voltage of the buffer is 100 mV, which is the worst case. The value of Ve is the maximum error voltage which is acceptable.

For a maximum error voltage (Ve) of 10 µV in the CS5505 (1/4LSB at 16-bits) and 600 nV in the CS5506 (1/4LSB at 20-bits), the above equation indicates that when operating from a 32.768 kHz XIN, source resistances up to 110 kΩ in the CS5505 or 84 kΩ in the CS5506 are acceptable in the absence of external capacitance (C_{EXT} = 0). If higher input source resistances are desired the master clock rate can be reduced to yield a longer settling time.

The VREF+ and VREF- inputs have nearly the same structure as the AIN+ and AIN- inputs. Therefore, the discussion on analog input impedance applies to the voltage reference inputs as well.

Digital Filter Characteristics

The digital filter in the CS5505/6/7/8 is the combination of a comb filter and a low pass filter. The comb filter has zeros in its transfer function which are optimally placed to reject line interference frequencies (50 and 60 Hz and their multiples) when the CS5505/6/7/8 is clocked at 32.768 kHz. Figures 9, 10 and 11 illustrate the magnitude and phase characteristics of the filter.

Figure 9 illustrates the filter attenuation from dc to 260 Hz. At exactly 50, 60, 100, and 120 Hz the filter provides over 120 dB of rejection. Table 3 indicates the filter attenuation for each of the potential line interference frequencies when the converter is operating with a 32.768 kHz clock. The converter yields excellent attenuation of these interference frequencies even if the fundamental line frequency should vary ±1% from its specified frequency. The -3 dB corner frequency of the filter when operating from a 32.768 kHz clock is 17 Hz. Figure 11 illustrates that the phase characteristics of the filter are precisely linear phase.

Figure 9. Filter Magnitude Plot to 260 Hz

Frequency (Hz)	Notch Depth (dB)	Frequency (Hz)	Minimum Attenuation (dB)
50	125.6	50±1%	55.5
60	126.7	60±1%	58.4
100	145.7	100±1%	62.2
120	136.0	120±1%	68.4
150	118.4	150±1%	74.9
180	132.9	180±1%	87.9
200	102.5	200±1%	94.0
240	108.4	240±1%	104.4

Table 3. Filter Notch Attenuation (XIN = 32.768 kHz)
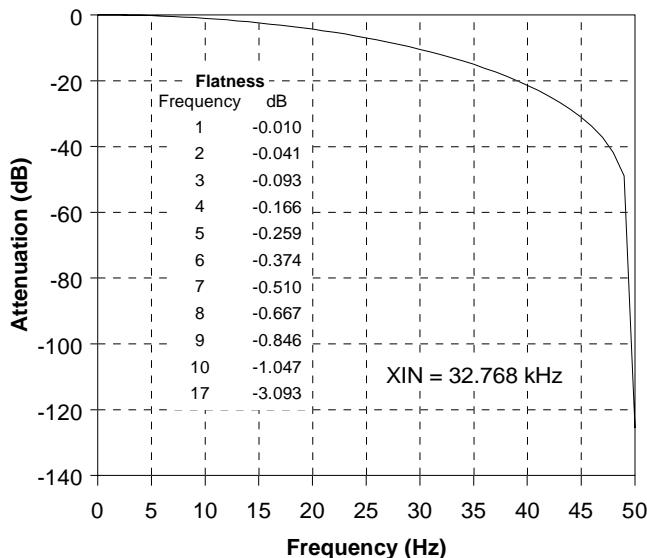
Figure 10. Filter Magnitude Plot to 50 Hz
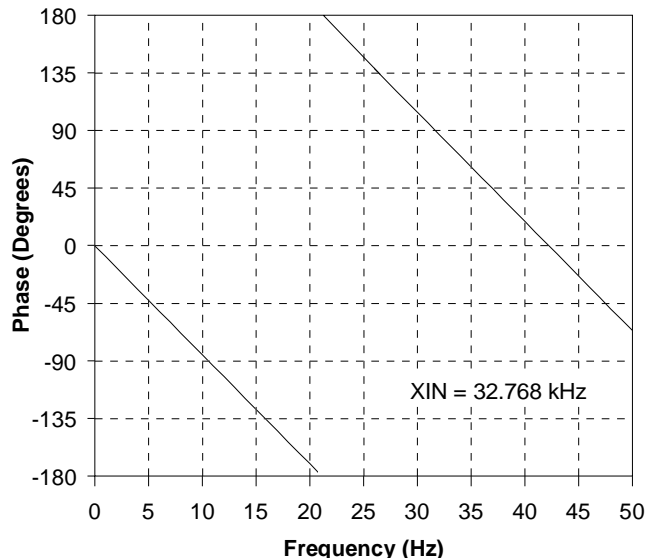
Figure 11. Filter Phase Plot to 50 Hz

If the CS5505/6/7/8 is operated at a clock rate other than 32.768 kHz, the filter characteristics, including the comb filter zeros, will scale with the operating clock frequency. Therefore, optimum rejection of line frequency interference will occur with the CS5505/6/7/8 running at 32.768 kHz. The CS5505/6/7/8 can be used with external clock rates from 30 kHz to 163 kHz.

Anti-Alias Considerations for Spectral Measurement Applications

Input frequencies greater than one half the output word rate (CONV = 1) may be aliased by the converter. To prevent this, input signals should be limited in frequency to no greater than one half the output word rate of the converter (when CONV =1). Frequencies close to the modulator sample rate (XIN/2) and multiples thereof may also be aliased. If the signal source includes spectral components above one half the output word rate (when CONV = 1) these com-

ponents should be removed by means of low-pass filtering prior to the A/D input to prevent aliasing. Spectral components greater than one half the output word rate on the VREF inputs (VREF+ and VREF-) may also be aliased. Filtering of the reference voltage to remove these spectral components from the reference voltage is desirable.

Crystal Oscillator

The CS5505/6/7/8 is designed to be operated using a 32.768 kHz "tuning fork" type crystal. One end of the crystal should be connected to the XIN input. The other end should be attached to XOUT. Short lead lengths should be used to minimize stray capacitance. Figure 12 illustrates the gate oscillator, and a simplified version of the control logic used on the chip.

Over the industrial temperature range (-40 to +85 °C) the on-chip gate oscillator will oscillate
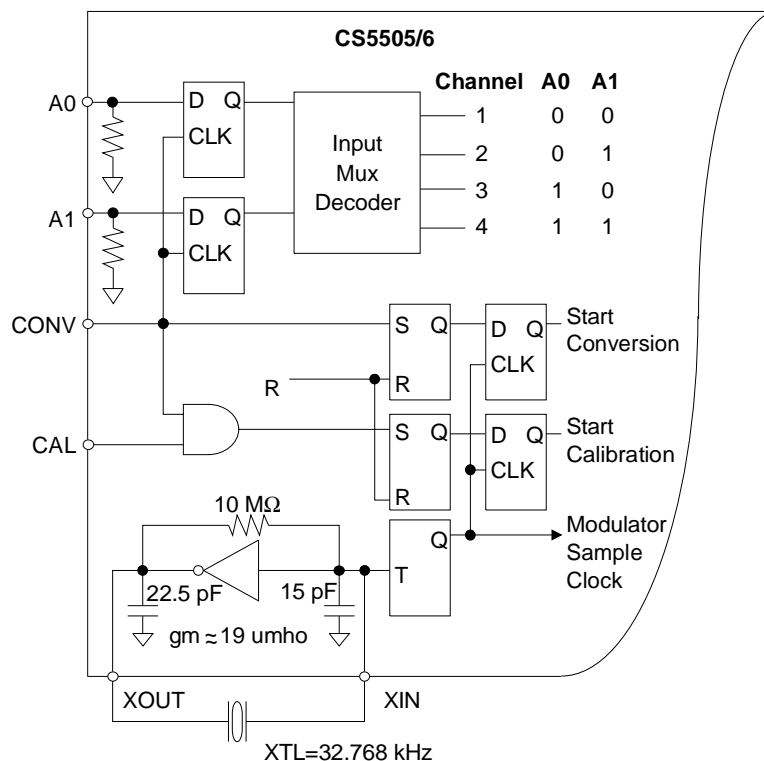
Figure 12. Gate Oscillator and Control Logic

with other crystals in the range of 30 kHz to 53 kHz.

The chip will operate with external clock frequencies from 30 kHz to 163 kHz. The 32.768 kHz crystal is normally specified as a time-keeping crystal with tight specifications for both initial frequency and for drift over temperature. To maintain excellent frequency stability, these crystals are specified only over limited operating temperature ranges (i.e. -10 to +60 °C) by the manufacturers. Applications of these crystals with the CS5505/6/7/8 do not require tight initial tolerance or low tempco drift. Therefore, a lower cost crystal with looser initial tolerance and tempco will generally be adequate for use with the CS5505/6/7/8 converters. Also check with the manufacturer about wide temperature range application of their standard crystals. Generally, even those crystals specified for limited temperature range will operate over much larger ranges if frequency stability over temperature is not a requirement. The frequency stability can be as bad as ±3000 ppm over the operating temperature range and still be typically better than the line frequency (50 or 60 Hz) stability over cycle to cycle during the course of a day.

Serial Interface Logic

The digital filter in the CS5505/6/7/8 takes 1624 clock cycles to compute an output word once a conversion begins. At the end of the conversion cycle, the filter will attempt to update the serial port. Two clock cycles prior to the update $\overline{DRDY}$ will go high. When $\overline{DRDY}$ goes high just prior to a port update it checks to see if the port is either empty or unselected ($\overline{CS}$ = 1). If the port is empty or unselected, the digital filter will update the port with a new output word.

When new data is put into the port $\overline{DRDY}$ will go low.

Data can be read from the serial port in either of two modes. The M/SLP pin determines which serial mode is selected. Serial port mode selection is as follows:

SSC (Synchronous Self-Clocking) mode; M/SLP = VD+, or SEC (Synchronous External Clocking) mode; M/SLP = DGND. Timing diagrams which illustrate the SSC and SEC timing are in the tables section of this data sheet.

Synchronous Self-Clocking Mode

The serial port operates in the SSC mode when the M/SLP pin is connected to the VD+ pin on the part. In SSC mode the CS5505/6/7/8 furnishes both the serial output data (SDATA) and the serial clock (SCLK). When the serial port is updated at the end of a conversion, $\overline{DRDY}$ falls. If $\overline{CS}$ is low, the SDATA and SCLK pins will come out of the high impedance state two XIN clock cycles after $\overline{DRDY}$ falls. The MSB data bit will be presented for two cycles of XIN clock. The SCLK signal will rise in the middle of the MSB data bit. When SCLK then returns low the (MSB - 1) bit will appear. Subsequent data bits will be output on each falling edge of SCLK until the LSB data bit is output. After the LSB data bit is output, the SCLK will fall at which time both the SDATA and SCLK outputs will return to the high impedance output state. $\overline{DRDY}$ will return high at this time.

If $\overline{CS}$ is taken low after $\overline{DRDY}$ falls, the MSB data bit will appear within two XIN clock cycles after $\overline{CS}$ is taken low. $\overline{CS}$ need not be held low for the entire data output. If $\overline{CS}$ is returned high during a data bit the port will complete the output of that bit and then go into the Hi-Z state. The port can be reselected any time prior to the completion of the next conversion ($\overline{DRDY}$ falling) to allow the remaining data bits to be output.

Synchronous External-Clocking Mode

The serial port operates in the SEC mode when the M/SLP pin is connected to the DGND pin. SDATA is the output pin for the serial data. When $\overline{CS}$ goes low after new data becomes available ($\overline{DRDY}$ goes low), the SDATA pin comes out of Hi-Z with the MSB data bit present. SCLK is the input pin for the serial clock in the SEC mode. If the MSB data bit is on the SDATA pin, the first rising edge of SCLK enables the shifting mechanism. This allows the falling edges of SCLK to shift subsequent data bits out of the port. Note that if the MSB data bit is output and the SCLK signal is high, the first falling edge of SCLK will be ignored because the shifting mechanism has not become activated. After the first rising edge of SCLK, each subsequent falling edge will shift out the serial data. Once the LSB is present, the falling edge of SCLK will cause the SDATA output to go to Hi-Z and $\overline{DRDY}$ to return high. The serial port register will be updated with a new data word upon the completion of another conversion if the serial port has been emptied, or if the $\overline{CS}$ is inactive (high).

$\overline{CS}$ can be operated asynchronously to the $\overline{DRDY}$ signal. The $\overline{DRDY}$ signal need not be monitored as long as the $\overline{CS}$ signal is taken low for at least two XIN clock cycles plus 200 ns prior to SCLK being toggled. This ensures that $\overline{CS}$ has gained control over the serial port.

Sleep Mode

The CS5505/6/7/8 devices offer two methods of putting the device into a SLEEP condition to conserve power. Calibration words will be retained in SRAM during either sleep condition. The M/SLP pin can be put into the SLEEP threshold to lower the operating power used by the device to about 1% of nominal. Alternately, the clock into the XIN pin can be stopped. This will lower the power consumed by the converter to about 30% of nominal. In both cases, the

converter must go through a wake-up sequence prior to conversions being initiated. This wake-up sequence includes the 10 msec. (typ.) power-on-reset delay, the start-up of the oscillator (unless an external clock is used), and the 1800 clock cycle wake-up delay after the clock begins. When coming out of the sleep condition, the converter will latch the A0 and A1 inputs.

Figure 13 illustrates how to use a gate and resistors to bias the M/SLP pin into the SLEEP threshold region when using the converter in the SSC mode. To use the SEC mode return resistor R1 to DGND instead of the supply. When in the SEC mode configuration the CS5505/6/7/8 will enter the SLEEP threshold when the logic control input is a logic 1 (VD+). Note that large resistors can be used to conserve power while in sleep. The input leakage of the pin is typically less than 1 µA even at 125 °C, although the worst case specification tables indicate a leakage
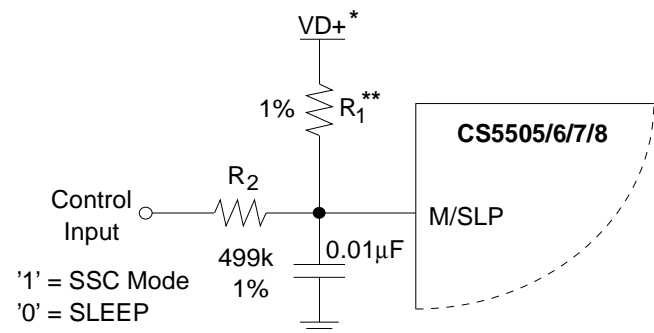
* Tie R_1 to DGND for SEC mode; control input logic inverts.

** R_1 = 499k, V_D+ = 5V; R_1 = 590k, V_D+ = 3.3V

Figure 13. Sleep Threshold Control

of 10 µA maximum.

Power Supplies and Grounding

The analog and digital supply pins to the CS5505/6/7/8 are brought out on separate pins to minimize noise coupling between the analog and digital sections of the chip. Note that there is no

analog ground pin. No analog ground pin is required because the inputs for measurement and for the voltage reference are differential and require no ground. In the digital section of the chip the supply current flows into the VD+ pin and out of the DGND pin. As a CMOS device, the CS5505/6/7/8 requires that the supply voltage on the VA+ pin always be more positive than the voltage on any other pin of the device. If this requirement is not met, the device can latch-up or be damaged. In all circumstances the VA+ voltage must remain more positive than the

VD+ or DGND pins; VD+ must remain more positive than the DGND pin.

The following power supply options are possible:

VA+ = +5V to +10V,   VA- = 0V,   VD+ = +5V
VA+ = +5V,   VA- = -5V,   VD+ = +5V
VA+ = +5V,   VA- = 0V to -5V,   VD+ = +3.3V

The CS5505/6/7/8 cannot be operated with a 3.3V digital supply if VA+ is greater than +5.5V.
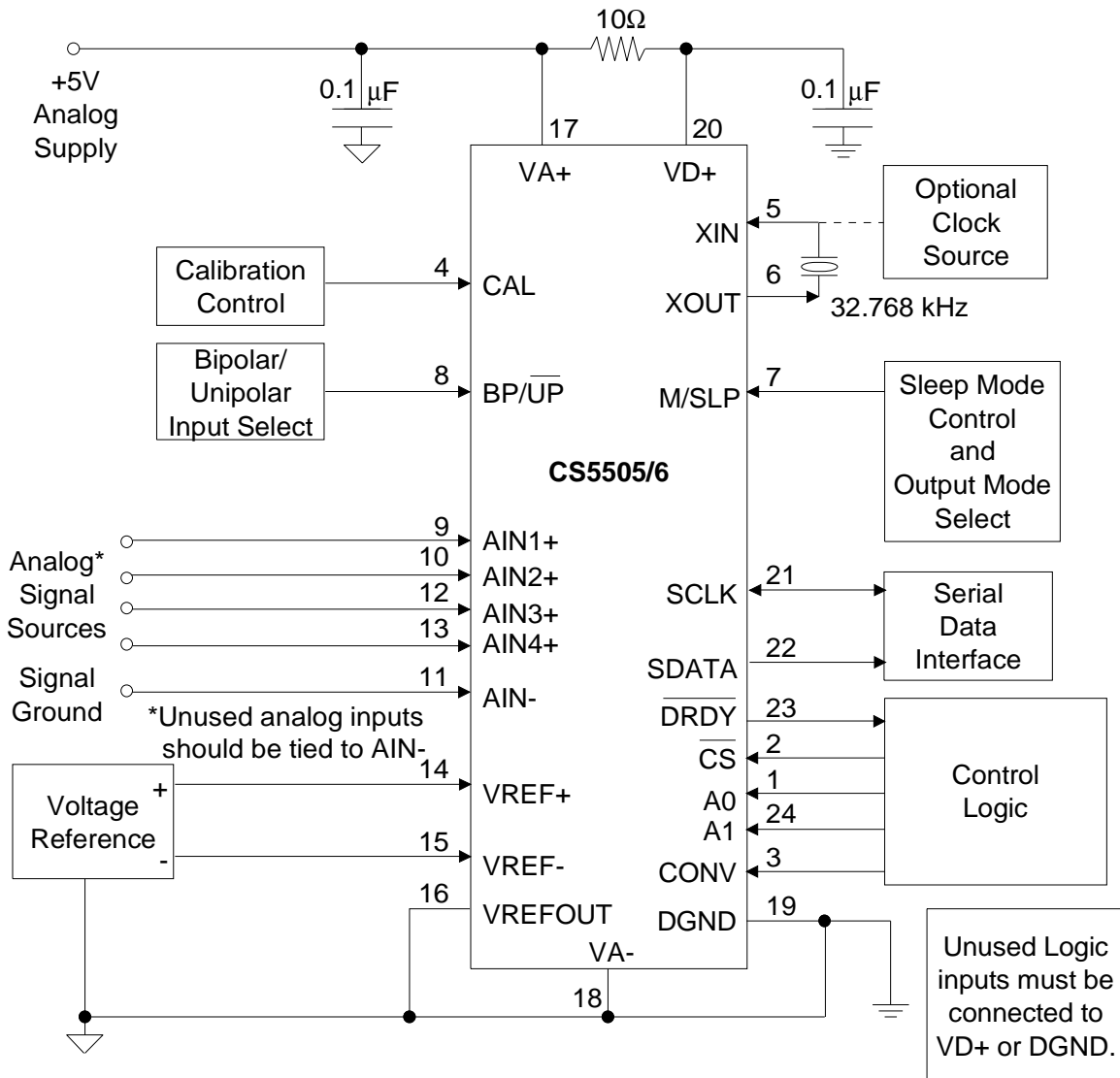
Note: To use the internal 2.5 volt reference see Figure 6.

Figure 14. CS5505/6 System Connection Diagram Using External Reference, Single Supply

Figure 15 illustrates the CS5505/6 using dual supplies of +5 and -5V.

under any operating condition. Remember to investigate transient power-up conditions, when one power supply may have a faster rise time.
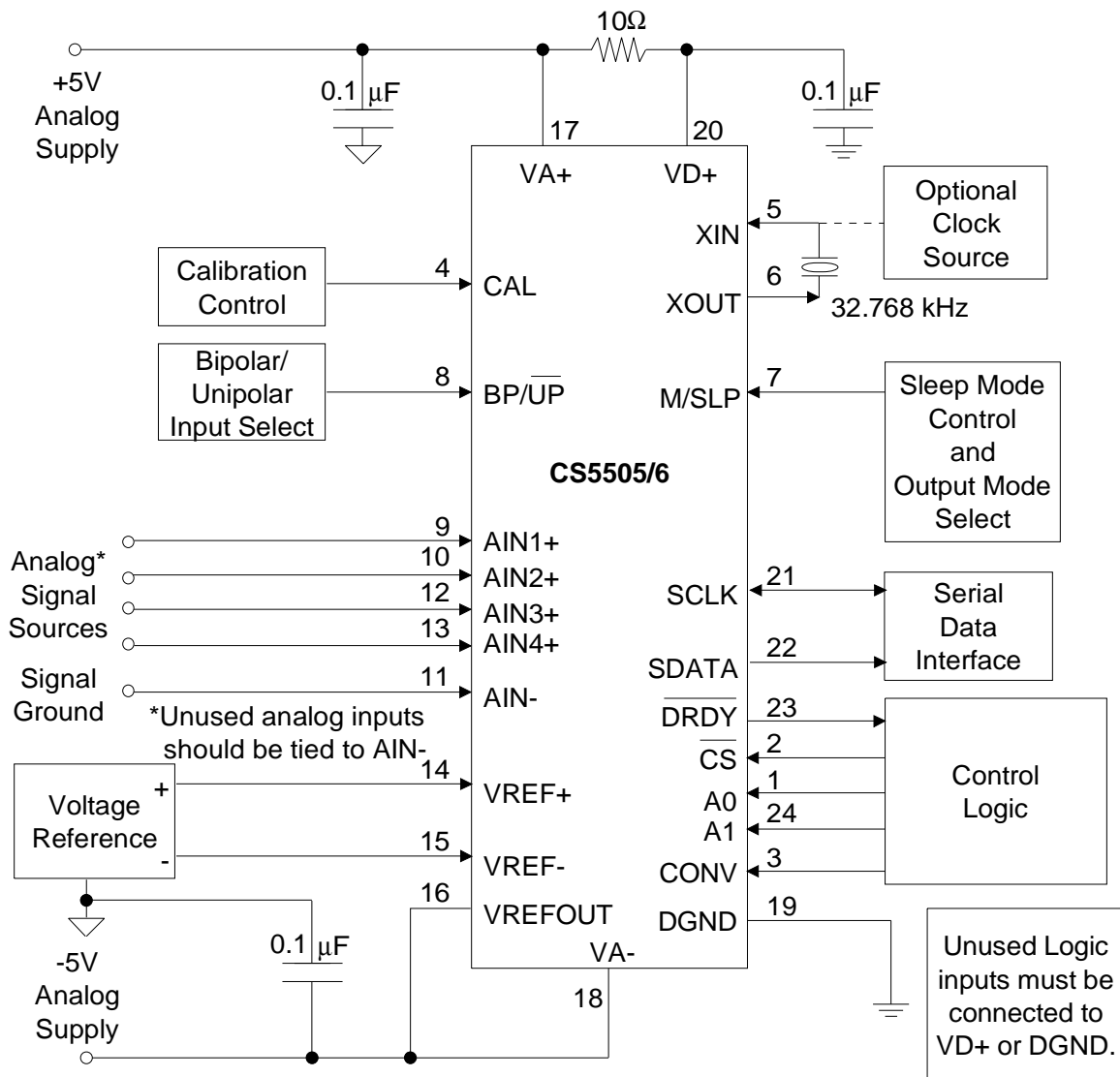
Note: To use the internal 2.5 volt reference see Figure 6.

Figure 15. CS5505/6 System Connection Diagram Using External Reference, Dual Supplies

Figure 16. CS5505/6 System Connection Diagram Using External Reference, Dual Supply, +10V Analog, +5V Digital
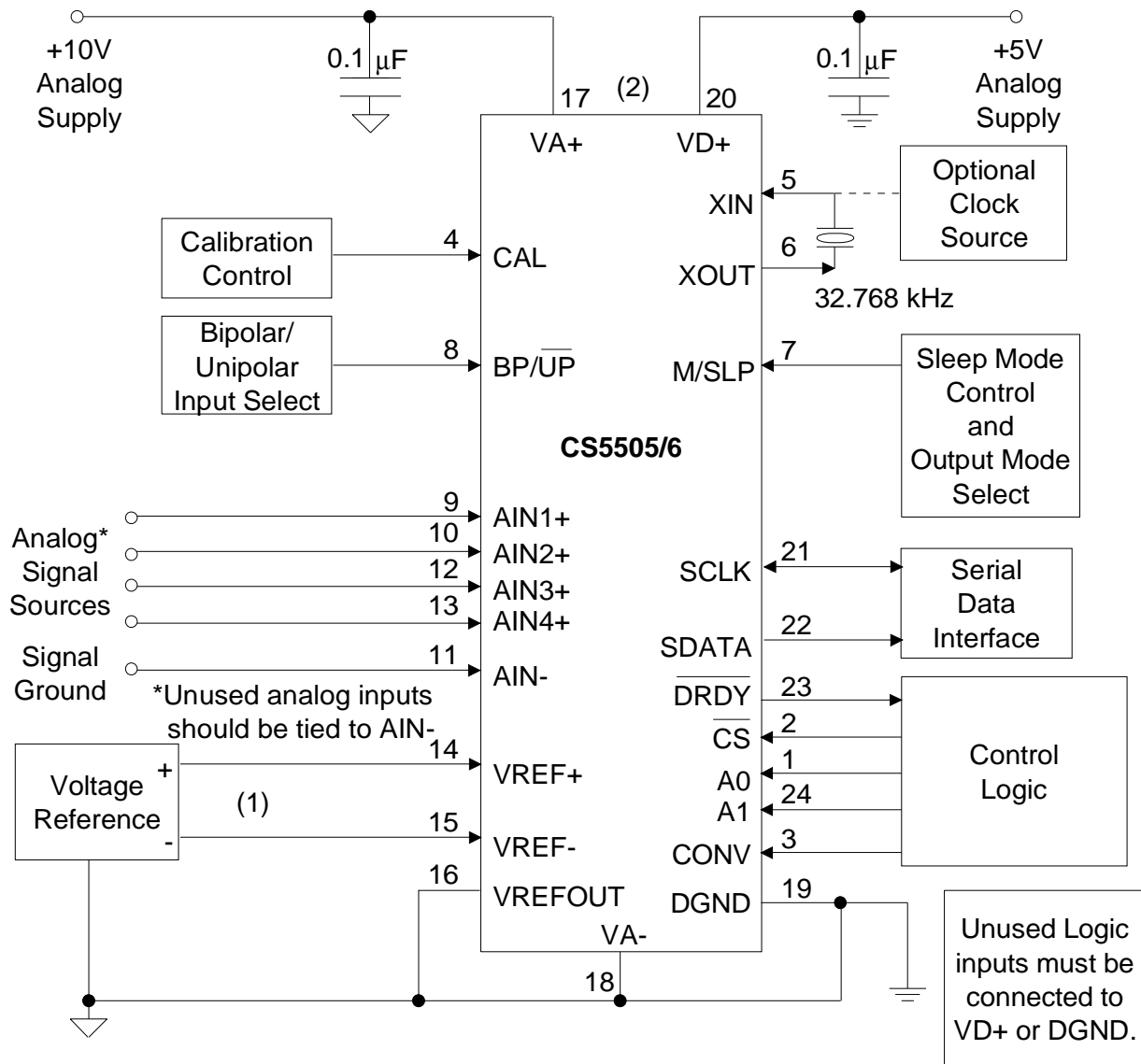
Note: (1) To use the internal 2.5 volt reference see Figure 6.
(2) VD+ must never exceed VA+. Examine power-up conditions.

PIN CONNECTIONS*

CS5505/6

MULTIPLEXER SELECTION INPUT	**A0**	1	24	**A1**	MULTIPLEXER SELECTION INPUT
CHIP SELECT	**$\overline{CS}$**	2	23	**$\overline{DRDY}$**	DATA READY
CONVERT	**CONV**	3	22	**SDATA**	SERIAL DATA OUTPUT
CALIBRATE	**CAL**	4	21	**SCLK**	SERIAL CLOCK INPUT/OUTPUT
CRYSTAL IN	**XIN**	5	20	**VD+**	POSITIVE DIGITAL POWER
CRYSTAL OUT	**XOUT**	6	19	**DGND**	DIGITAL GROUND
SERIAL MODE/ SLEEP	**M/SLP**	7	18	**VA-**	NEGATIVE ANALOG POWER
BIPOLAR/UNIPOLAR	**BP/$\overline{UP}$**	8	17	**VA+**	POSITIVE ANALOG POWER
DIFFERENTIAL ANALOG INPUT	**AIN1+**	9	16	**VREFOUT**	VOLTAGE REFERENCE OUTPUT
DIFFERENTIAL ANALOG INPUT	**AIN2+**	10	15	**VREF-**	VOLTAGE REFERENCE INPUT
DIFFERENTIAL ANALOG RETURN	**AIN-**	11	14	**VREF+**	VOLTAGE REFERENCE INPUT
DIFFERENTIAL ANALOG INPUT	**AIN3+**	12	13	**AIN4+**	DIFFERENTIAL ANALOG INPUT

CS5507/8

CHIP SELECT	**$\overline{CS}$**	1	20	**$\overline{DRDY}$**	DATA READY
CONVERT	**CONV**	2	19	**SDATA**	SERIAL DATA OUTPUT
CALIBRATE	**CAL**	3	18	**SCLK**	SERIAL CLOCK INPUT/OUTPUT
CRYSTAL IN	**XIN**	4	17	**VD+**	POSITIVE DIGITAL POWER
CRYSTAL OUT	**XOUT**	5	16	**DGND**	DIGITAL GROUND
SERIAL MODE/ SLEEP	**M/SLP**	6	15	**VA-**	NEGATIVE ANALOG POWER
BIPOLAR/UNIPOLAR	**BP/$\overline{UP}$**	7	14	**VA+**	POSITIVE ANALOG POWER
DIFFERENTIAL ANALOG INPUT	**AIN+**	8	13	**VREFOUT**	VOLTAGE REFERENCE OUTPUT
NO CONNECTION	**NC**	9	12	**VREF-**	VOLTAGE REFERENCE INPUT
DIFFERENTIAL ANALOG INPUT	**AIN-**	10	11	**VREF+**	VOLTAGE REFERENCE INPUT

*Pinout applies to both DIP and SOIC

PIN DESCRIPTIONS

Pin numbers for four channel devices are in parentheses.

Clock Generator

XIN; XOUT - Crystal In; Crystal Out, Pins 4 (5) and 5 (6).

A gate inside the chip is connected to these pins and can be used with a crystal to provide the master clock for the device. Alternatively, an external (CMOS compatible) clock can be supplied into the XIN pin to provide the master clock for the device. Loss of clock will put the device into a lower powered state (approximately 70% power reduction).

Serial Output I/O

M/SLP - Serial Interface Mode Select/ Sleep, Pin 6 (7).

Dual function pin which selects the operating mode of the serial port and provides a very low power sleep function. When M/SLP is tied to the VD+ pin the serial port will operate in the Synchronous Self-Clocking (SSC) mode. When M/SLP is tied to the DGND pin the serial port will operate in the Synchronous External Clocking (SEC) mode. When the M/SLP pin is tied half way between VD+ and DGND the chip will enter into a very low powered sleep mode in which its calibration data will be maintained.

$\overline{\text{CS}}$ **- Chip Select, Pin 1 (2).**

This input allows an external device to access the serial port.

$\overline{\text{DRDY}}$ **- Data Ready, Pin 20 (23)**

Data Ready goes low at the end of a digital filter convolution cycle to indicate that a new output word has been placed into the serial port. $\overline{\text{DRDY}}$ will return high after all data bits are shifted out of the serial port or two master clock cycles before new data becomes available if the $\overline{\text{CS}}$ pin is inactive (high).

SDATA - Serial Data Output, Pin 19 (22).

SDATA is the output pin of the serial output port. Data from this pin will be output at a rate determined by SCLK and in a format determined by the M/SLP pin. Data is output MSB first and advances to the next data bit on the falling edges of SCLK. SDATA will be in a high impedance state when not transmitting data.

SCLK - Serial Clock Input/Output, Pin 18 (21).

A clock signal on this pin determines the output rate of the data from the SDATA pin. The M/SLP pin determines whether SCLK is an input or and output. When used as an input, it must not be allowed to float.

Control Input Pins

CAL - Calibrate, Pin 3 (4).
When taken high the same time that the CONV pin is taken high the converter will perform a self-calibration which includes calibration of the offset and gain scale factors in the converter.

CONV - Convert, Pin 2 (3).
The CONV pin initiates a calibration cycle if it is taken from low to high while the CAL pin is high, or it initiates a conversion if it is taken from low to high with the CAL pin low. CONV latches the multiplexer selection when it transitions from low to high on the multiple channel devices. If CONV is held high (CAL low) the converter will do continuous conversions.

A0, A1 - Multiplexer Selection Inputs, Pins (1, 24).
A0 and A1 select the input channel for conversion on the multi-channel input devices. A0 and A1 are latched when CONV transitions from low to high. These two inputs have pull-down resistors internal to the chip.

BP/$\overline{\text{UP}}$ - Bipolar/Unipolar, Pin 7 (8).
The BP/$\overline{\text{UP}}$ pin selects the conversion mode of the converter. When high the converter will convert bipolar input signals; when low it will convert unipolar input signals.

Measurement and Reference Inputs

AIN+, AIN-, (AIN1+, AIN2+, AIN3+, AIN4+, AIN-) - Differential Analog Inputs, Pins 8, 10 (9, 10, 12, 13, 11).
AIN- in the CS5505/6 is a common measurement node for AIN1+, AIN2+, AIN3+ and AIN4+.

VREF+, VREF- - Differential Voltage Reference Inputs, Pins 11, 12 (14, 15).
A differential voltage reference on these pins operates as the voltage reference for the converter. The voltage between these pins can be any voltage between 1.0 and 3.6 volts.

Voltage Reference

VREFOUT - Voltage Reference Output, Pin 13 (16).
The on-chip voltage reference is output from this pin. The voltage reference has a nominal magnitude of 2.5 volts and is referenced to the VA+ pin on the converter.

Power Supply Connections

VA+ - Positive Analog Power, Pin 14 (17).
Positive analog supply voltage. Nominally +5 volts.

VA- - Negative Analog Power, Pin 15 (18).
Negative analog supply voltage. Nominally -5 volts when using dual polarity supplies; or 0 volts (tied to system analog ground) when using single supply operation.

VD+ - Positive Digital Power, Pin 17 (20).
> Positive digital supply voltage. Nominally +5 volts or 3.3 volts.

DGND - Digital Ground, Pin 16 (19).
> Digital Ground.

Other

NC - No Connection, Pin 9.
> Pin should be left floating.

SPECIFICATION DEFINITIONS

Linearity Error
> The deviation of a code from a straight line which connects the two endpoints of the A/D Converter transfer function. One endpoint is located 1/2 LSB below the first code transition and the other endpoint is located 1/2 LSB beyond the code transition to all ones. Units in percent of full-scale.

Differential Nonlinearity
> The deviation of a code's width from the ideal width. Units in LSBs.

Full Scale Error
> The deviation of the last code transition from the ideal [{(VREF+) - (VREF-)} - $\frac{3}{2}$ LSB]. Units are in LSBs.

Unipolar Offset
> The deviation of the first code transition from the ideal ($\frac{1}{2}$ LSB above the voltage on the AIN-pin.) when in unipolar mode (BP/$\overline{\text{UP}}$ low). Units are in LSBs.

Bipolar Offset
> The deviation of the mid-scale transition (011...111 to 100...000) from the ideal ($\frac{1}{2}$ LSB below the voltage on the AIN- pin.) when in bipolar mode (BP/$\overline{\text{UP}}$ high). Units are in LSBs

ORDERING INFORMATION

Model	Package	Resolution	Liearity Error	Channels	Temperature
CS5505-AP	24-pin Plastic DIP	16 Bits	0.0030%	4	-40 to +85 °C
CS5505-AS	24-pin SOIC				
CS5505-ASZ (lead free)					
CS5506-BP	24-pin Plastic DIP	20 Bits	0.0015%		
CS5506-BS	24-pin SOIC				
CS5506-BSZ (lead free)					
CS5507-AP	20-pin Plastic DIP	16 Bits	0.0030%	1	
CS5507-AS	20-pin SOIC				
CS5507-ASZ (lead free)					
CS5508-BP	20-pin Plastic DIP	20 Bits	0.0015%		
CS5508-BS	20-pin SOIC				
CS5508-BSZ (lead free)					

ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS5505-AP	260 °C	1	No Limit
CS5505-AS	240 °C	2	365 Days
CS5505-ASZ (lead free)	260 °C	3	7 Days
CS5506-BP	260 °C	1	No Limit
CS5506-BS	240 °C	2	365 Days
CS5506-BSZ (lead free)	260 °C	3	7 Days
CS5507-AP	260 °C	1	No Limit
CS5507-AS	240 °C	2	365 Days
CS5507-ASZ (lead free)	260 °C	3	7 Days
CS5508-BP	260 °C	1	No Limit
CS5508-BS	240 °C	2	365 Days
CS5508-BSZ (lead free)	260 °C	3	7 Days

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

REVISION HISTORY

Revision	Date	Changes
F4	MAR 1995	First Final Release
F5	AUG 2005	Updated device ordering info. Updated legal notice. Added MSL data..

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.

To find the one nearest to you go to www.cirrus.com

- NOTES -

CDB5505/6/7/8

Evaluation Board for CS5505/6/7/8 Series of ADCs

Features

- Operation with on-board 32.768 kHz crystal or off-board clock source
- Jumper selectable:
  - SSC mode; SEC mode; Sleep
- DIP Switch Selectable:
  - BP/$\overline{\text{UP}}$ mode; A0, & A1 channel selection
- On-board precision voltage reference
- Access to all digital control pins
- On-board patch area

Description

The CDB5505/5506/5507/5508 is a circuit board designed to provide quick evaluation of the CS5505/6/7/8 series of A/D converters. The board can be configured to evaluate the CS5505/6/7/8 in either SSC (Synchronous Self-Clocking) or SEC (Synchronous External-Clocking) serial port mode.

The board allows access to all of the digital interface pins of the CS5505/6/7/8 chip.

ORDERING INFORMATION

CDB5505	Evaluation Board
CDB5506	Evaluation Board
CDB5507	Evaluation Board
CDB5508	Evaluation Board
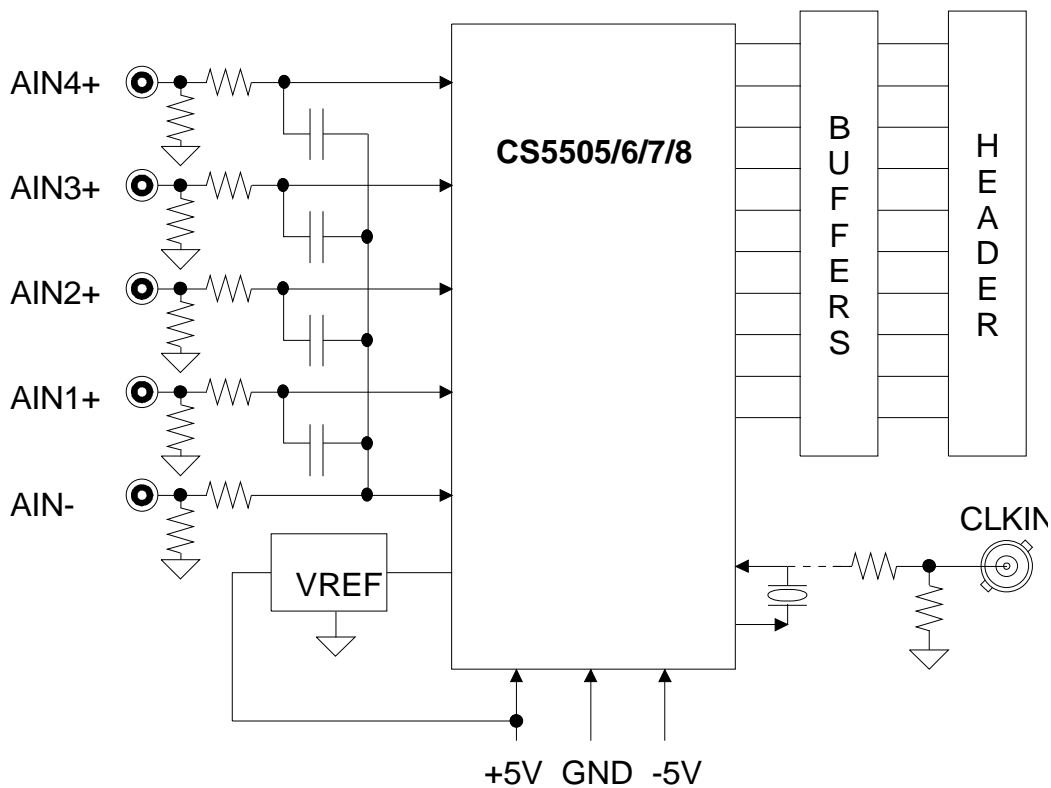
Introduction

The CDB5505/6/7/8 evaluation board provides a quick means of testing the CS5505/6/7/8 series A/D converters. The CS5505/6/7/8 converters require a minimal amount of external circuitry. The evaluation board comes configured with the A/D converter chip operating from a 32.768 kHz crystal and with an off-chip precision 2.5 volt reference. The board provides access to all of the digital interface pins of the CS5505/6/7/8 chip.

The board is configured for operation from +5 and -5 volt power supplies, but can be operated from a single +5 volt supply if the -5V binding post is shorted to the GND binding post.

Evaluation Board Overview

The board provides a complete means of making the CS5505/6/7/8 A/D converter chip function. The user must provide a means of taking the output data from the board in serial format and using it in his system.

Figure 1 illustrates the schematic for the board. The board comes configured for the A/D converter chip to operate from the 32.768 kHz watch crystal. A BNC connector for an external clock is provided on the board. To connect the external BNC source to the converter chip, a circuit trace must be cut. Then a jumper must be inserted in the proper holes to connect the XIN pin of the converter to the input line from the BNC. The BNC input is terminated with a 50Ω resistor. Remove this resistor if driving from a logic gate. See the schematic in Figure 1.

The board comes with the A/D converter VREF+ and VREF- pins hard-wired to the 2.5 volt bandgap voltage reference IC on the board. The VREF+ and VREF- pins can be connected to either the on chip reference or an off-board reference if the connections (2A and 2B) to the bandgap IC are cut.

Note that the pin-out of the CS5505/6/7/8 series chips allows the 20-pin single channel devices to be plugged into the 24-pin, four channel footprint. See Figure 2 which illustrates the footprint compatibility.

Prior to powering up the board, select the serial port operating mode with the appropriate jumper on the M/SLP header. The device can be operated in either the SSC (Synchronous Self-Clocking) or the SEC (Synchronous External Clocking) mode. See the device data sheet for an explanation of these modes.

All of the control pins of the CS5505/6/7/8 are available at the J1 header connector. Buffer ICs U2 and U3 are used to buffer the converter for interface to off-board circuits. The buffers are used on the evaluation board only because the exact loading and off-board circuitry is unknown. Most applications will not require the buffer ICs for proper operation.

To put the board in operation, select either bipolar or unipolar mode with DIP switch S2. Then press the CAL pushbutton after the board is powered up. This initiates calibration of the converter which is required before measurements can be taken.

To select an input channel on the four channel devices, use DIP switch S2 to select the inputs

A1	A0	Channel addressed
0	0	AIN1
0	1	AIN2
1	0	AIN3
1	1	AIN4

Table 1. Multiplexer Truth Table
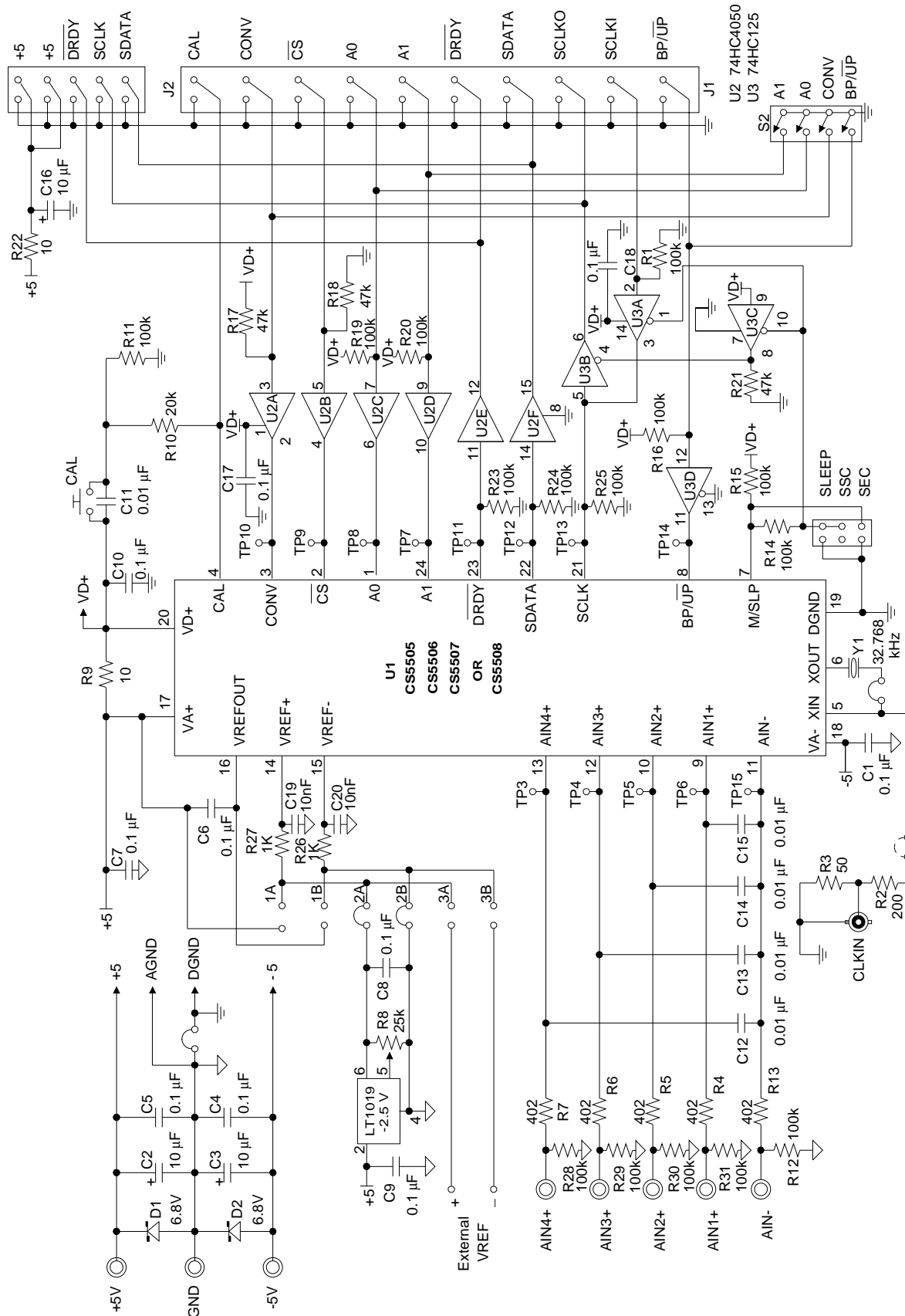
Figure 1. ADC Connections

CIRRUS LOGIC®

A0	1	CS5505/6	24	A1
CS	2/1		20/23	DRDY
CONV	3/2	CS5507/8	19/22	SDATA
CAL	4/3		18/21	SCLK
XIN	5/4		17/20	VD+
XOUT	6/5		16/19	DGND
M/SLP	7/6		15/18	VA-
BU/UP	8/7		14/17	VA+
AIN1+	9/8		13/16	VREFOUT
AIN2+/NC	10/9		12/15	VREF-
AIN-	11/10		11/14	VREF+
AIN3+	12		13	AIN4+
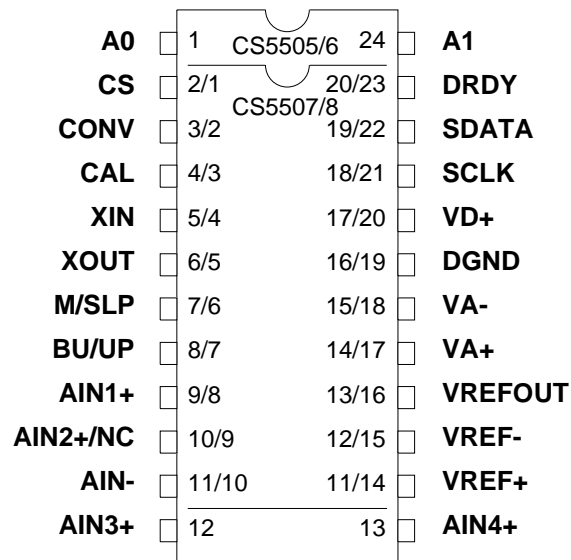
Figure 2. CS5505/6 and CS5507/8 Pin Layouts

for A0 and A1 (see Table 1). Once A0 and A1 are selected, the CONV switch (S2-3) must be switched on (closed) and then open to cause the CONV signal to transition low to high. This latches the A0 and A1 channel selection into the converter. With CONV high (S2-3 open) the converter will convert continuously.

Figures 3 and 4 illustrate the evaluation board layout while Figure 5 illustrates the component placement (silkscreen) of the evaluation board.
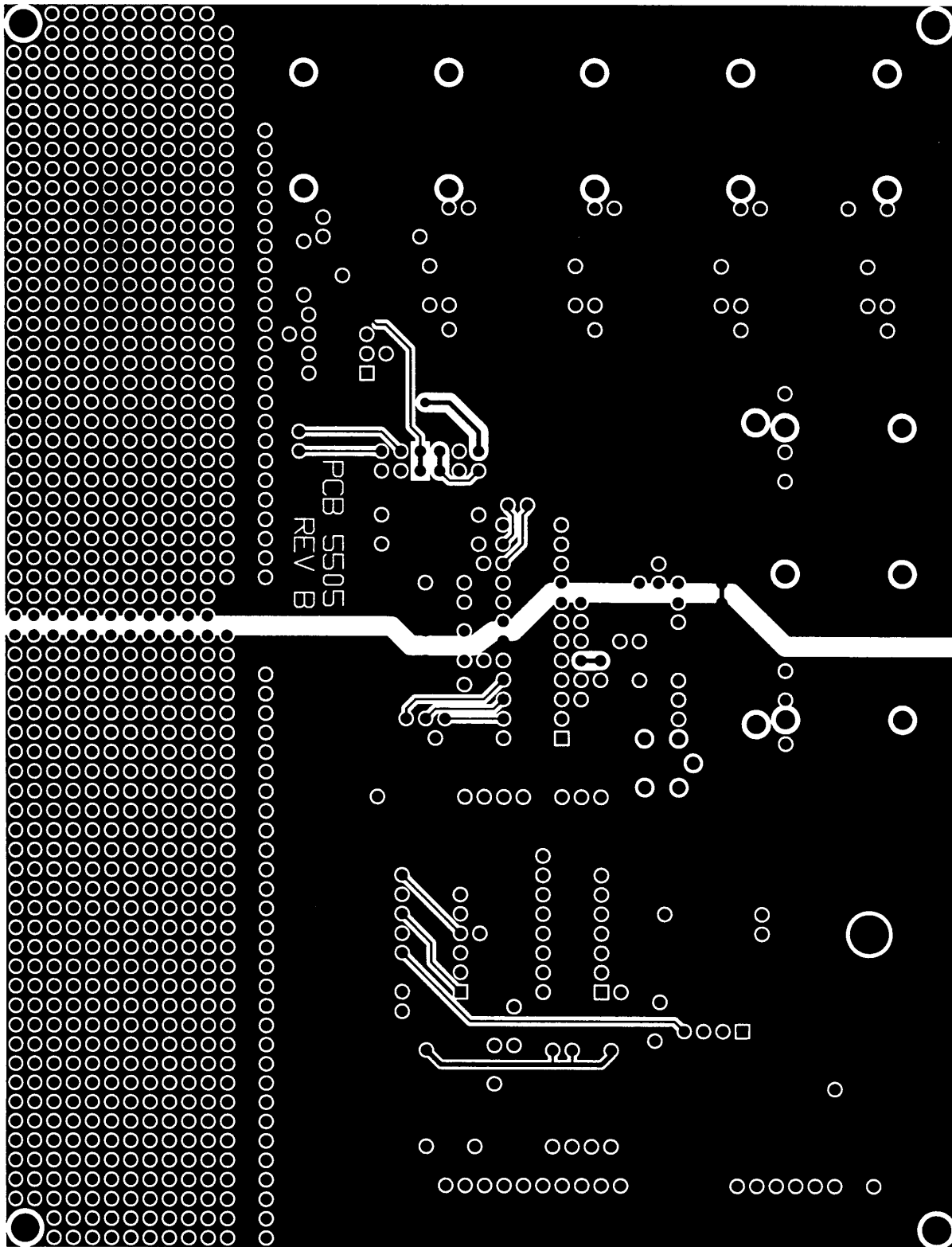
Figure 3. Top Ground Plane Layer (NOT TO SCALE)
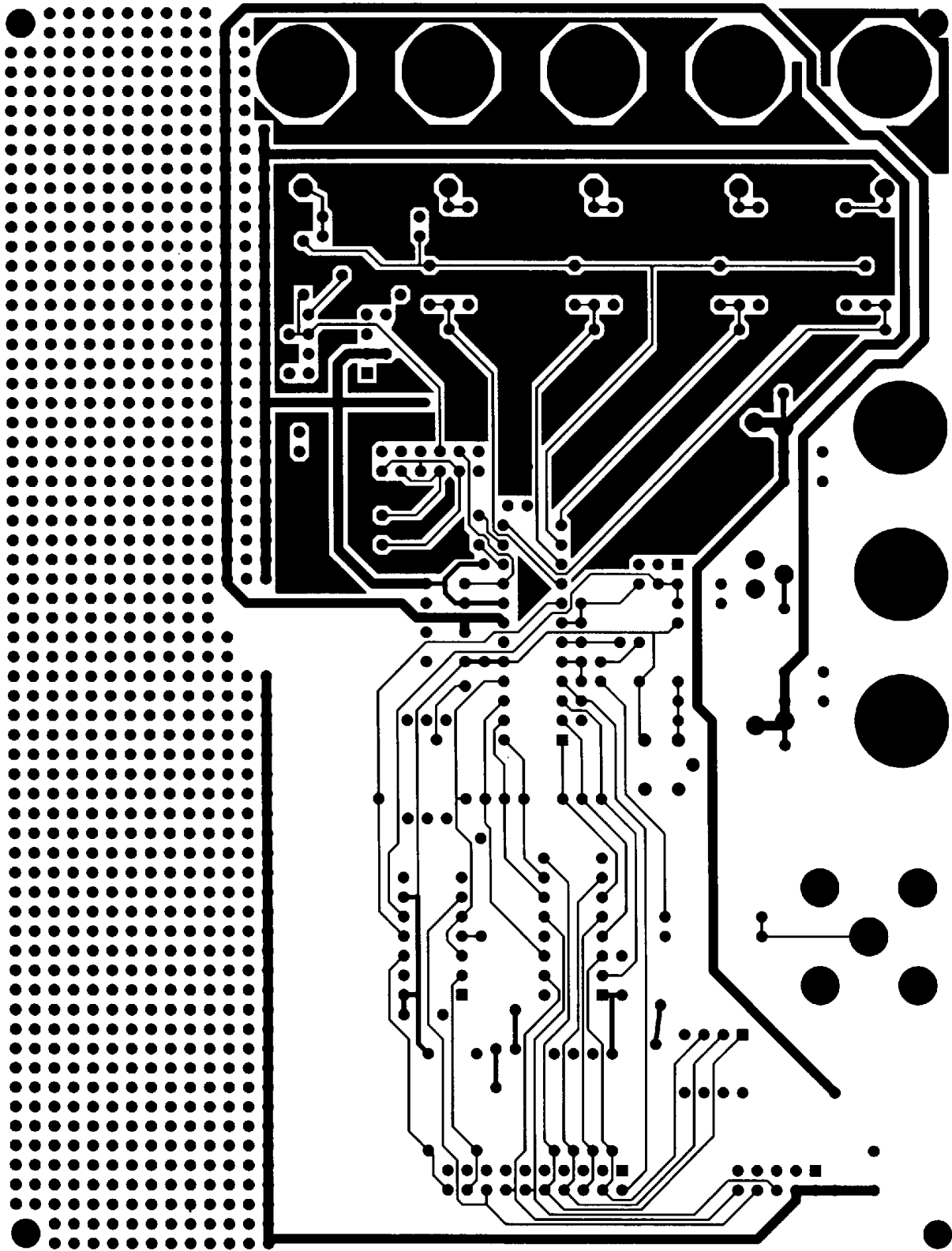
Figure 4. Bottom Trace Layer (NOT TO SCALE)
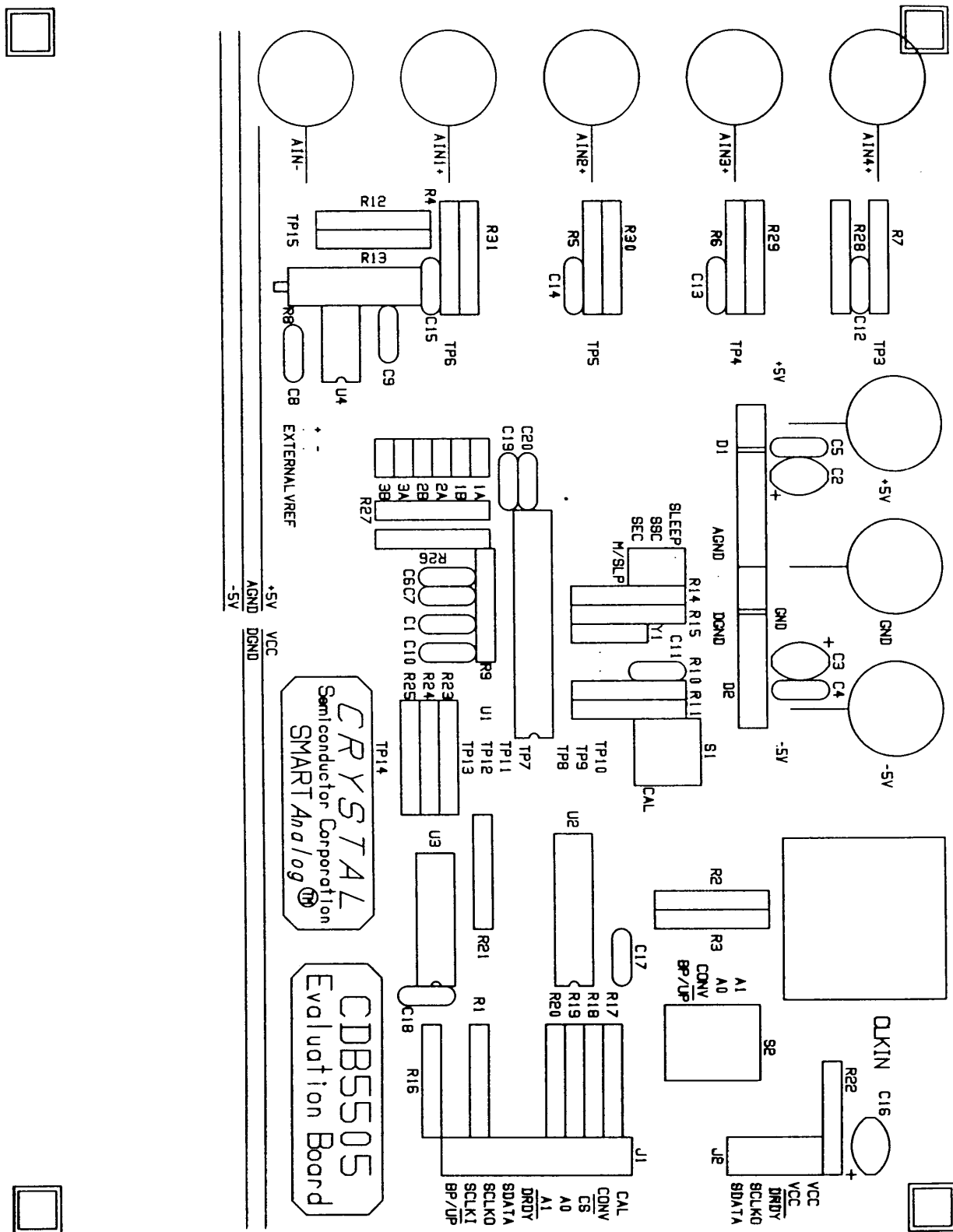
Figure 5. Silk Screen Layer (NOT TO SCALE)

REVISION HISTORY

Revision	Date	Changes
DB2	MAR 1995	First Release
F5	AUG 2005	Updated legal notice.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.

To find the one nearest to you go to www.cirrus.com